HDD Recorder DVR5100/75 & DVR7100/75

Service
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Service Manual

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GB 3139 785 32780

Version 1.0

PHILIPS

TABLE OF CONTENT

1. General

1. 1 Scope

This is the product sheet for the High-Definition (HD) Free to Air (FTA) MPEG2 Digital Video Recorder Set top box (STB) model DVR 5100/75 with 160GB HDD and DVR 7100/75 with 250GB HDD. This HD DVR is fully MPEG2 / DVB-T compliant, supporting channel frequencies range of 51 – 858MHz.

DVR 5100/75 and DVR 7100/75 is a custom made product for Philips Consumer Electronics, and has HDMI feature connectors for Digital Audio/Video output along with S-Video, YPbPr and Composite connectors.

1.2. Operating Conditions

Operating Temperature : +/- 0°C ~ +55°C

Before delivery of the product, the supplier shall submit the specification drawing, the sample, the test report and the QC (quality control) process flow chart to Philips Singapore.

2. Hardware Specification

System

Tuners: Two digital HD tuners (to receive digital transmission, see Basic Connection page 12-15)

Transmission standards: DVB-T

Channel coverage: 51 - 858 MHz. The above channel coverage merely ensures the channel reception within these ranges. It does not guarantee the ability to receive signals in all circumstances.

Aerial out: 75-ohm asymmetrical aerial socket

Video format: MP@ML, MP@HL

Audio format: Dolby Digital, MPEG (I and II)

Outputs

AUDIO OUT: RCA jacks (2 each)/2 Vrms/10 kilo ohms

VIDEO OUT: RCA jack/1.0 Vp-p/75 ohms

S VIDEO OUT: 4-pin mini DIN/Y:1.0 Vp-p,C: 0.3 Vp-p (PAL)/75 ohms

DIGITAL AUDIO OUT (OPTICAL): Opticaloutput jack/–18 dBm (wave length: 660 nm)

DIGITAL AUDIO OUT (COAXIAL): RCAjack/0.5 Vp-p/75 ohms

COMPONENT VIDEO OUT

(Y, PB/CB, PR/CR):

RCA jack/Y: 1.0 Vp-p, PB/CB: 0.7 Vp-p,

PR/CR: 0.7 Vp-p/75 ohms

HDMI OUT: Type A (19-pin)

General

Power requirements: 220-240 V AC, 50 Hz

Power consumption:

DVR 7100 : 30 W

DVR 5100 : 29 W

Dimensions (approx.): 430 _ 80 _ 290 mm

(width/height/depth) incl. projecting parts

Hard disk drive capacity:

DVR 7100 : 250GB

DVR 5100 : 160GB

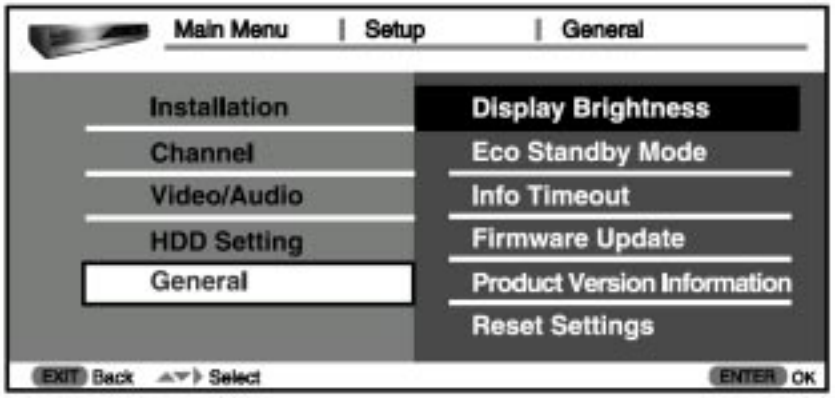
Mass (approx.): 4.0 kg

Operating temperature: 5ºC to 40ºC

Storage temperature: -40ºC to +65ºC

3. Adjustments & Settings :

3.1 Re-install the Set to Factory Settings after Repair:



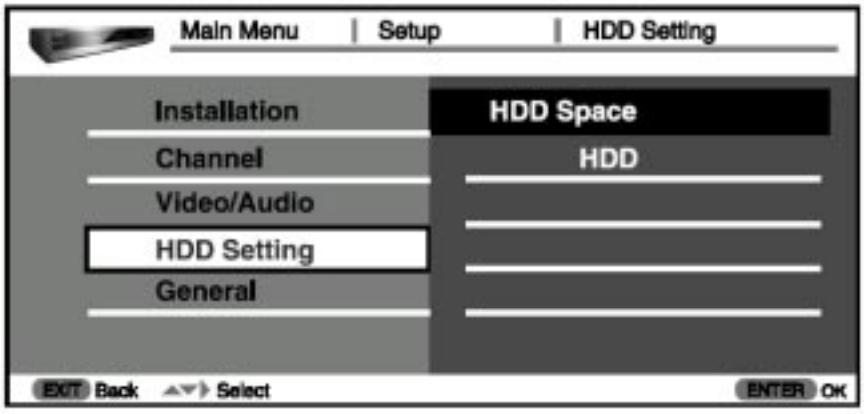
Goto Main Menu -> General -> Reset settings:

This feature enables you to return the setup settings to their defaults without affecting the recorded titles in the HDD.

Select { **Yes** }, and press **OK**.

The setup settings return to their defaults, and the recorder automatically turns off.

3.2 Re-format HDD:



Goto Main Menu -> HDD Setting -> Erase HDD:

Erases all the recorded titles in the HDD at once. Note that protected titles are also erased.

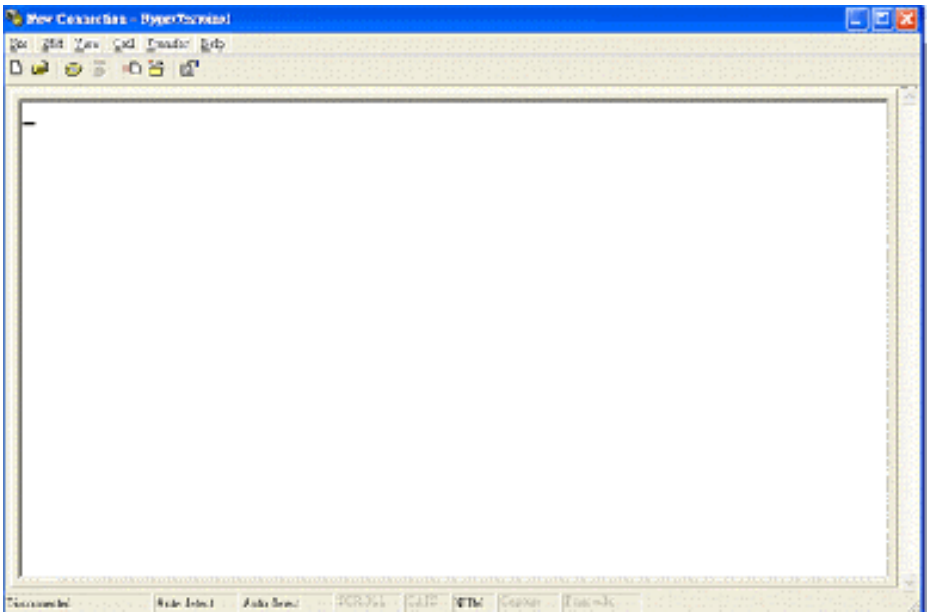
Press **OK** to confirm and press **BACK** to exit.

4. S/W UPGRADE PROCEDURE

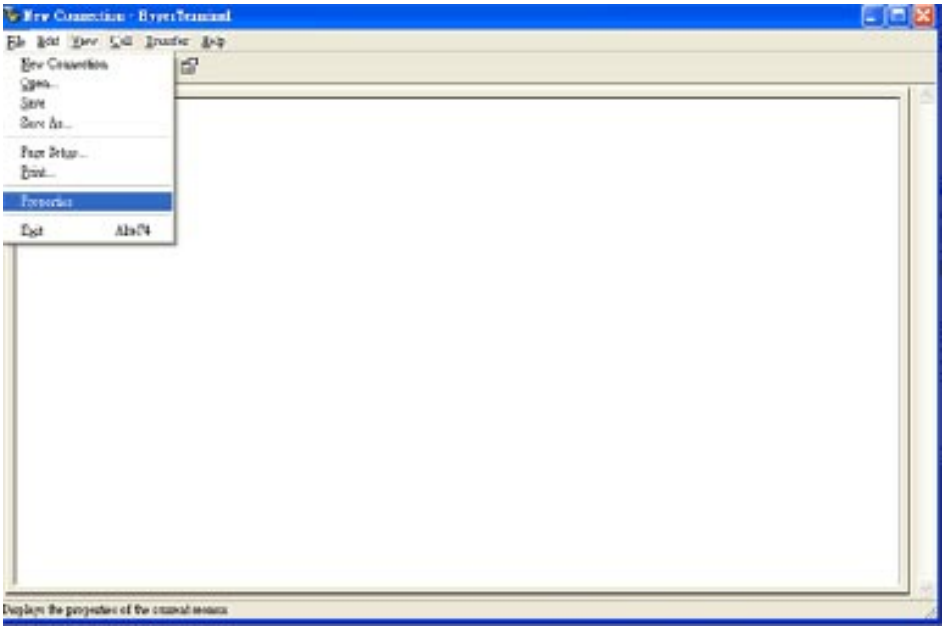
4.1 Use a crossover RS232 cable to connect ZINWELL Set-top Box and PC COM port.

4.2 On PC side:

Launch Hyperterminal in MS Windows, and set the parameters as follow “115200-N-8-N”. (It is in “Programs”-> “Accessories-> “Communication” -> “Hyperterminal”)

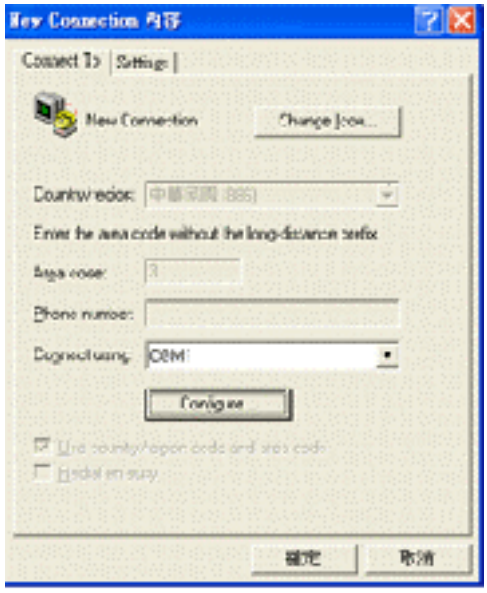


Enter the properties setting page:

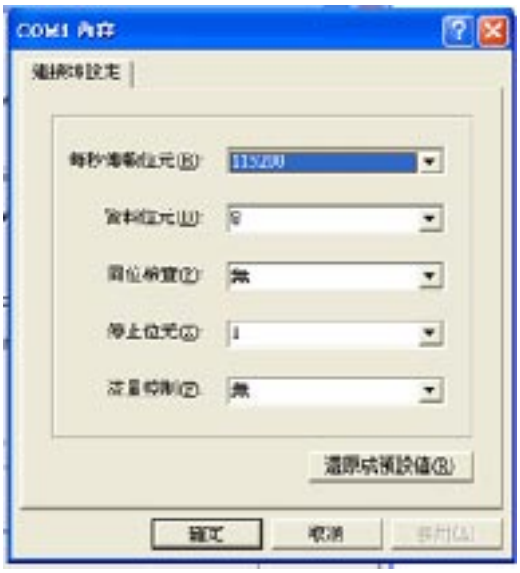


Set the COM port

Press Configure Button to Configure



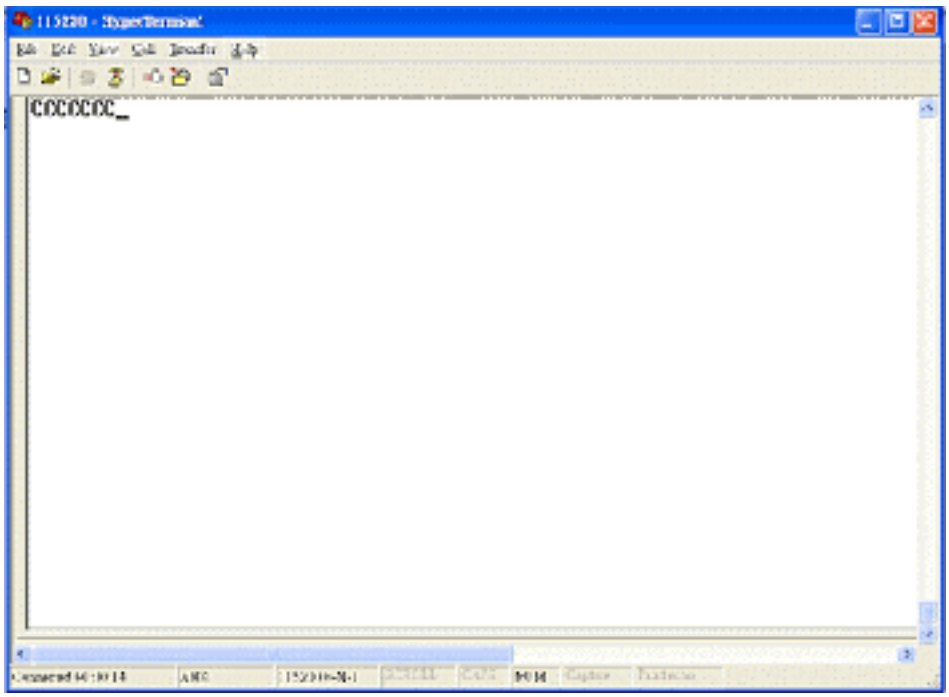
Setting the configure as following picture:



All settings are done. Press Call button to connect the Set-top box.

4.3 On Set-top box side:

Use OSD to upgrade s/w. Then you see “C C C C ...” shown on PC Hyperterminal screen.



4.5 On PC side:

Enter Hyper terminal menu, “ Transfer” -> “Send file” -> “BROWSE”, and select new software file (set protocol in 1K Xmodem)-> press “Send”

Ps. Set-top-box will wait PC to transmit the s/w. If you doesn’t send file to box, it will timeout then exit the upgrade status. You should redo these actions again.

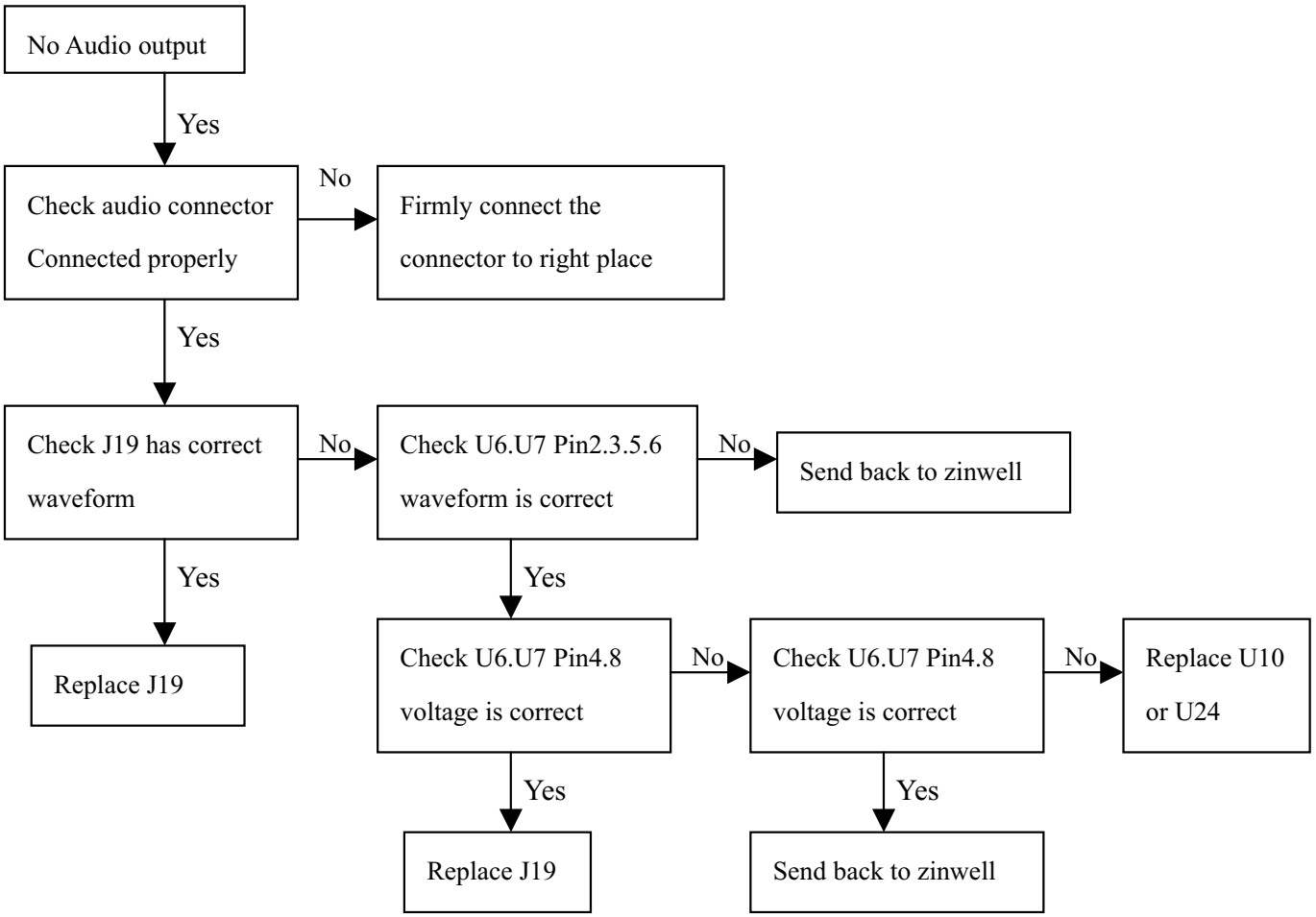
“Transfer” -> “Send file” -> “BROWSE”, and select new software file (set protocol in 1K Xmodem)-> press “Send”

6. When s/w update completed, the box will shut down automatically.

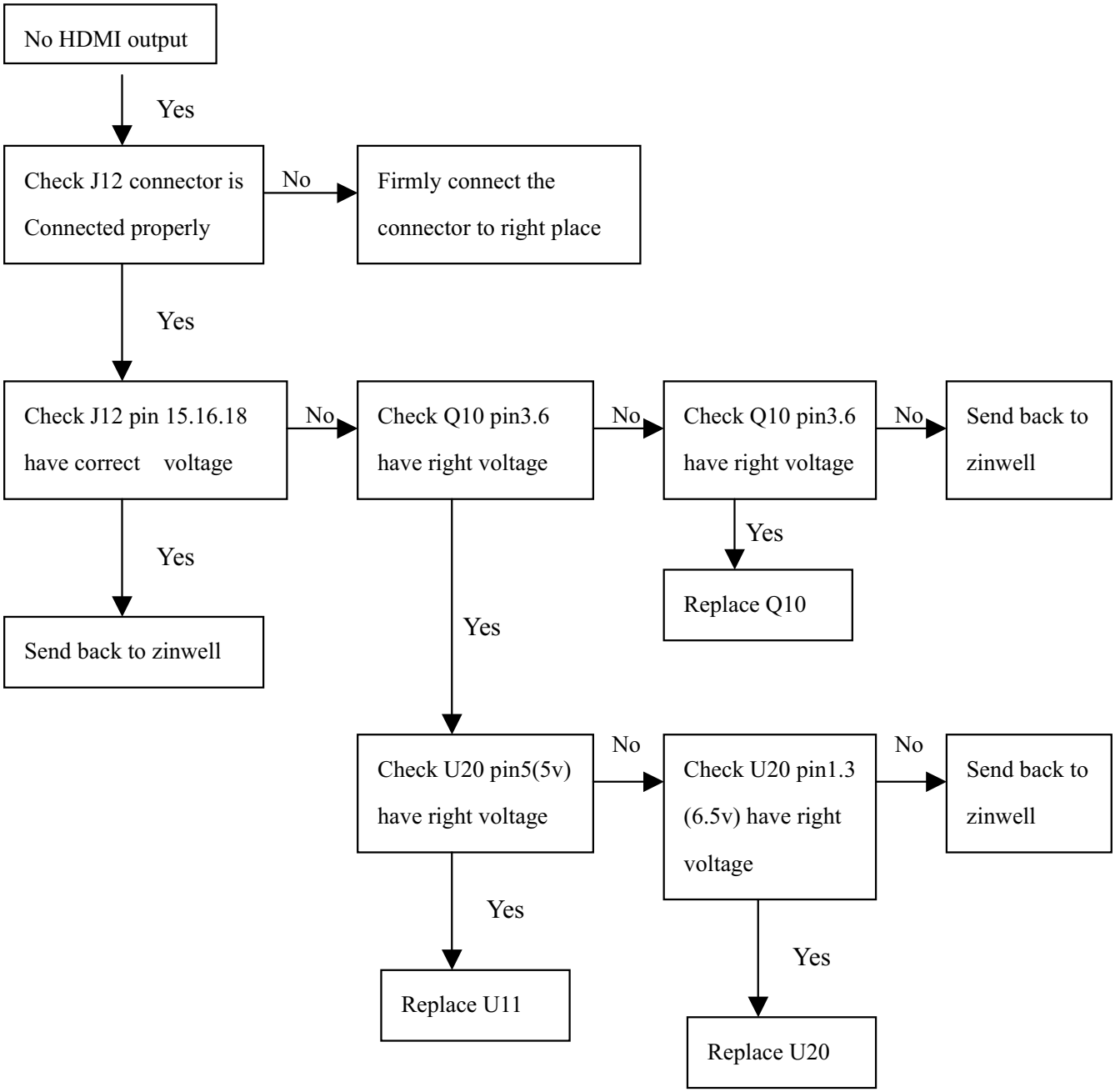
7. Restart box, it will boot up with new software.

5. Troubleshooting Flowchart

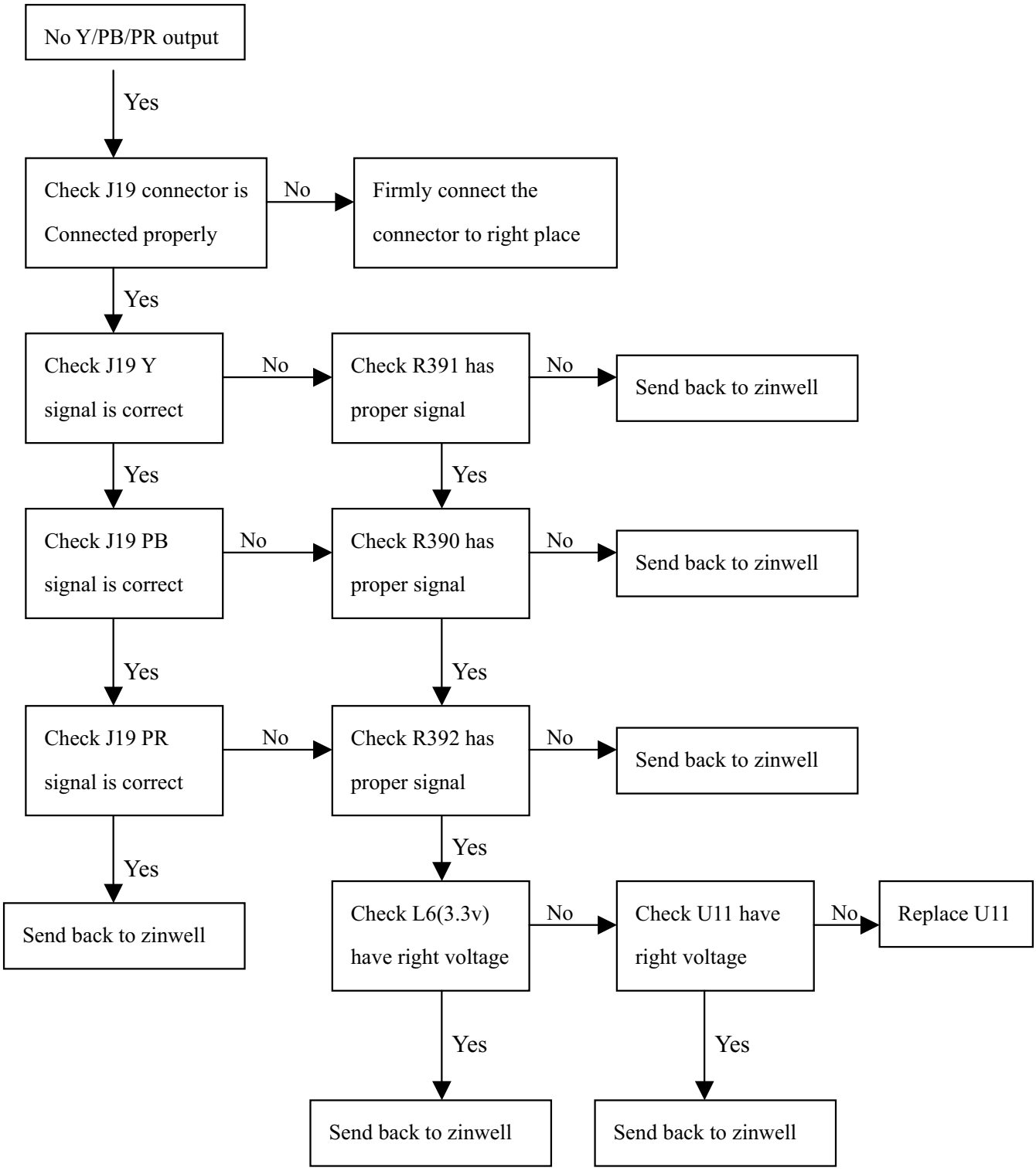
1. No Audio output : Flow chart



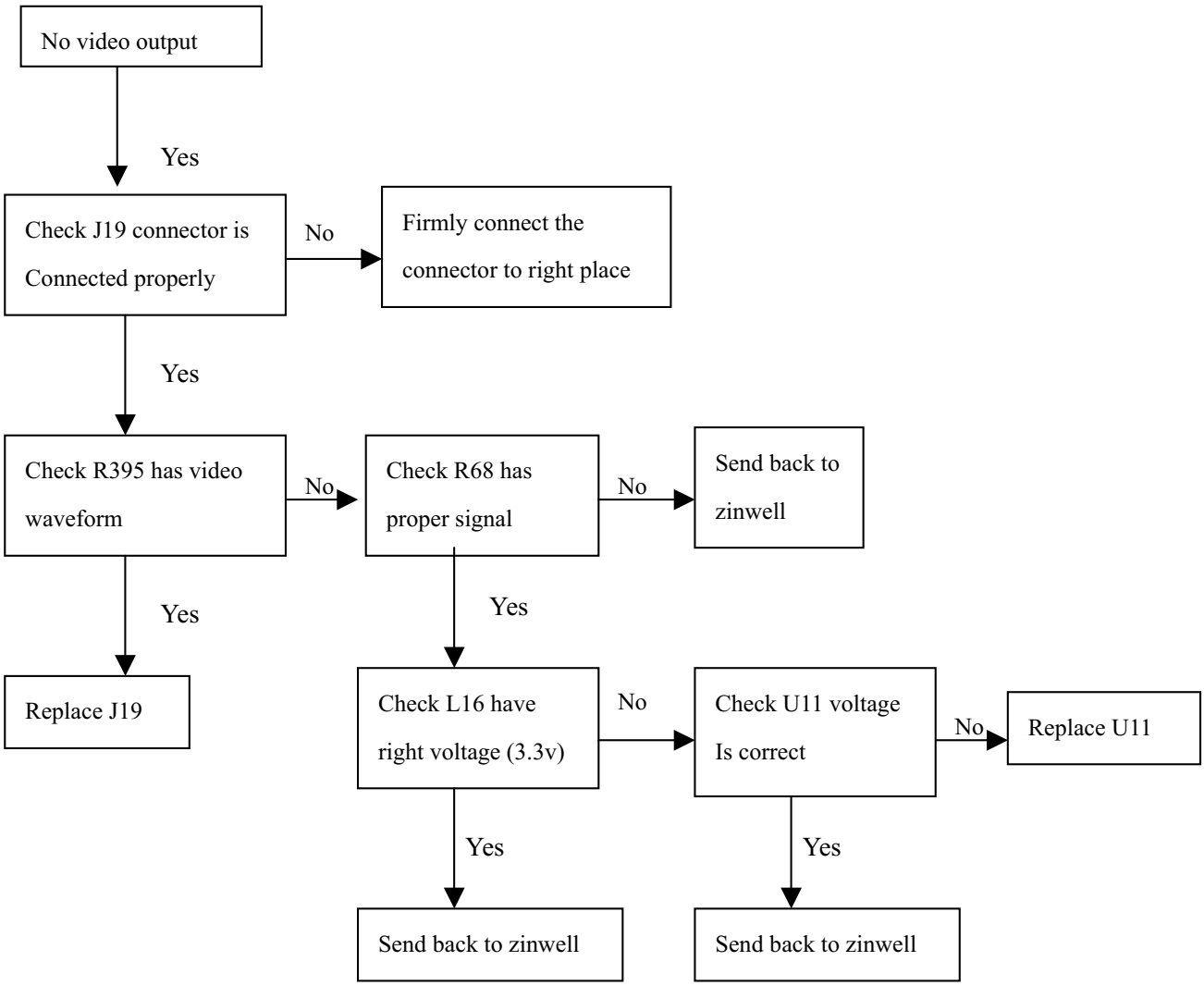
2. No HDMI output : Flow chart



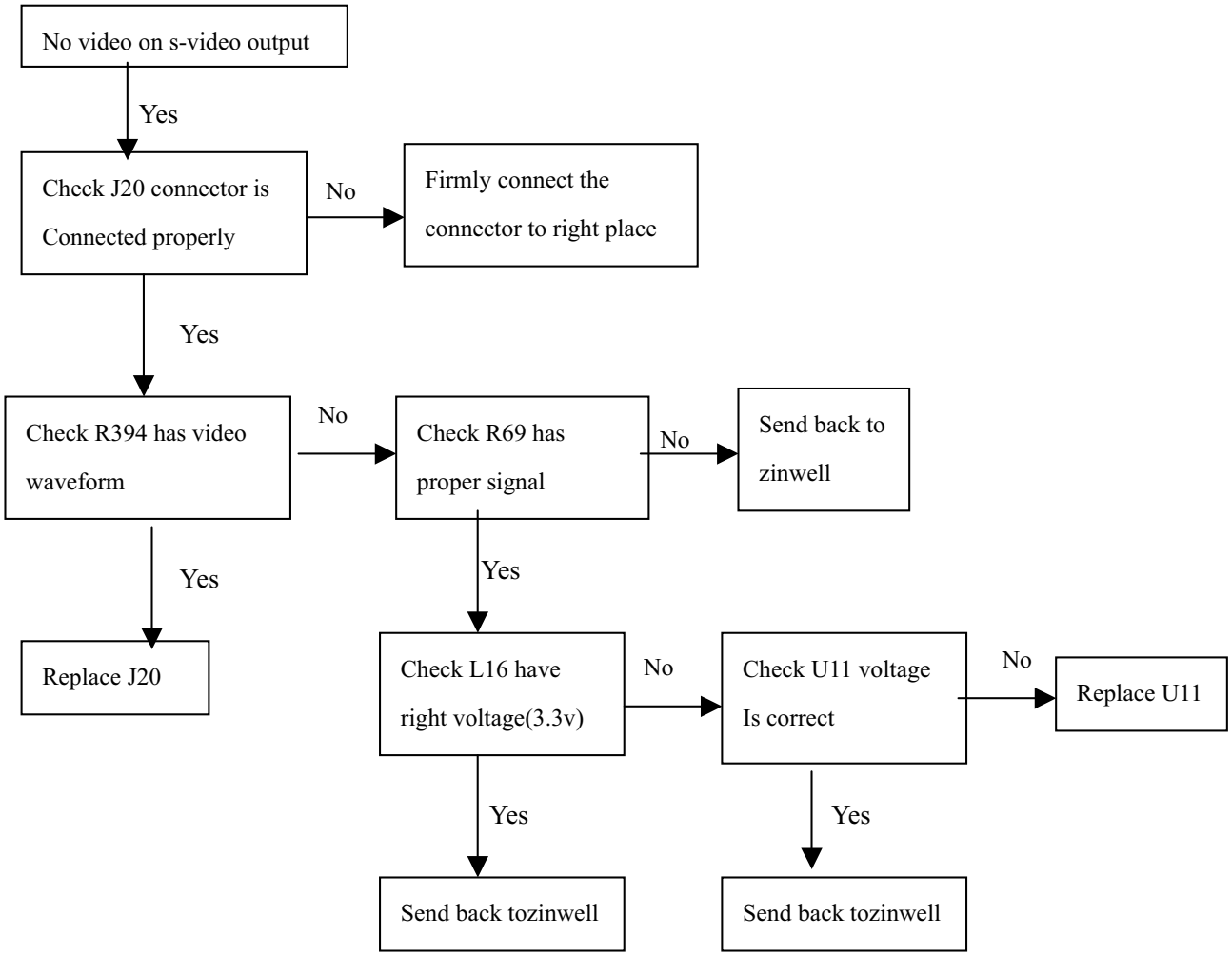
3. No Y/PB/PR output: Flow chart



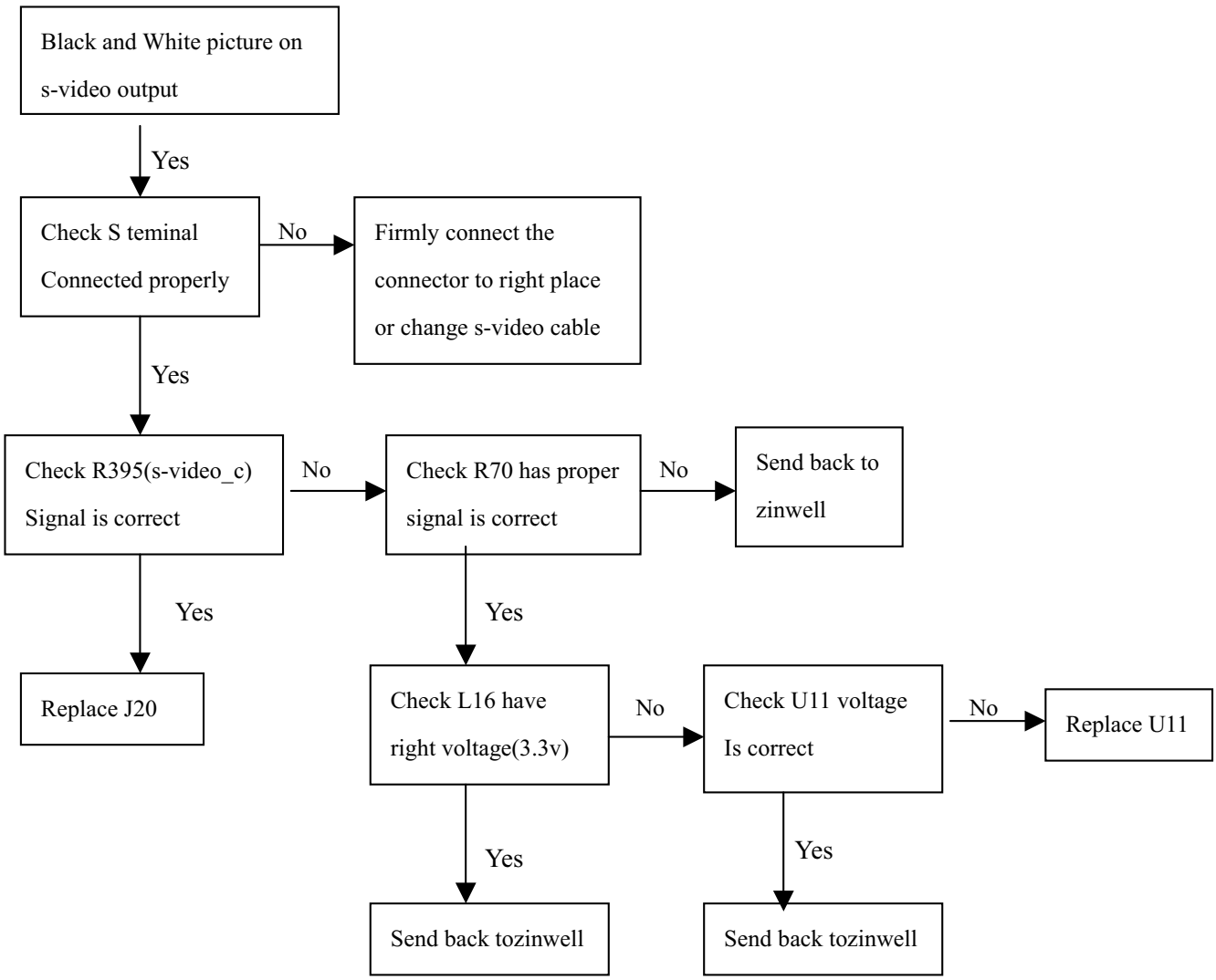
4. No Video output : Flow chart



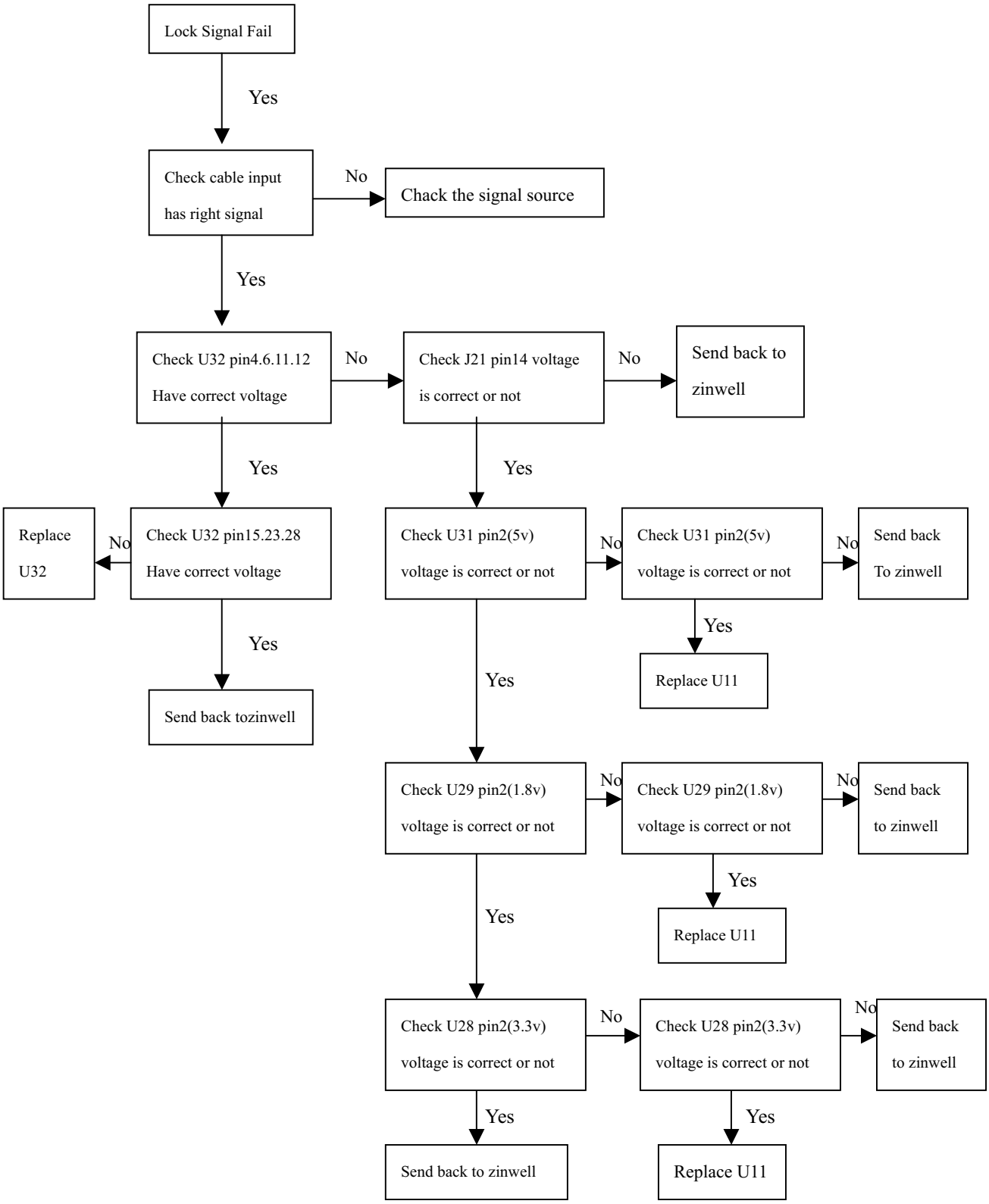
5. No Video on S-video output : Flow chart



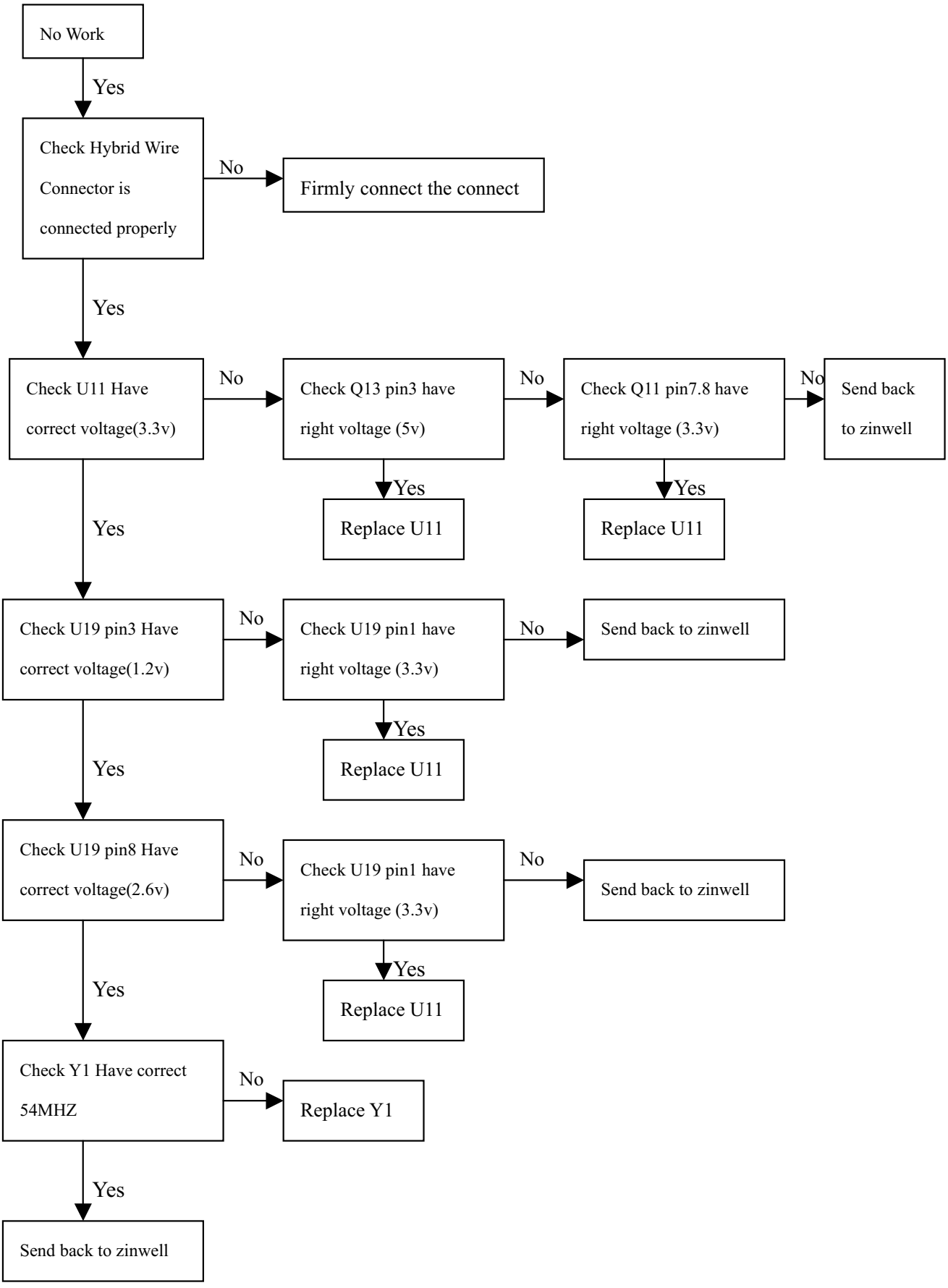
6. Black and White picture on S-video output : Flow chart



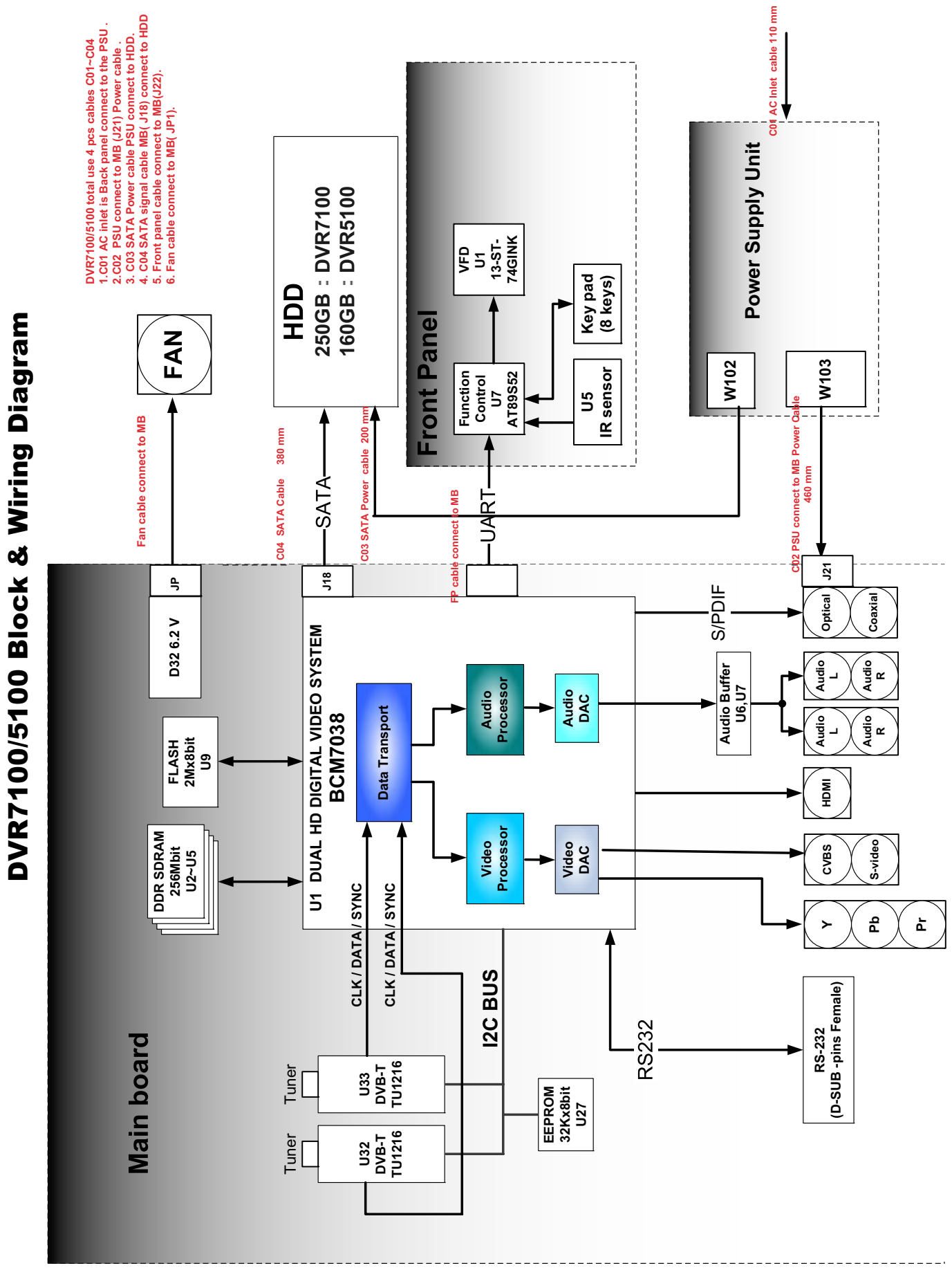
7. Lock Signal Fail : Flow chart



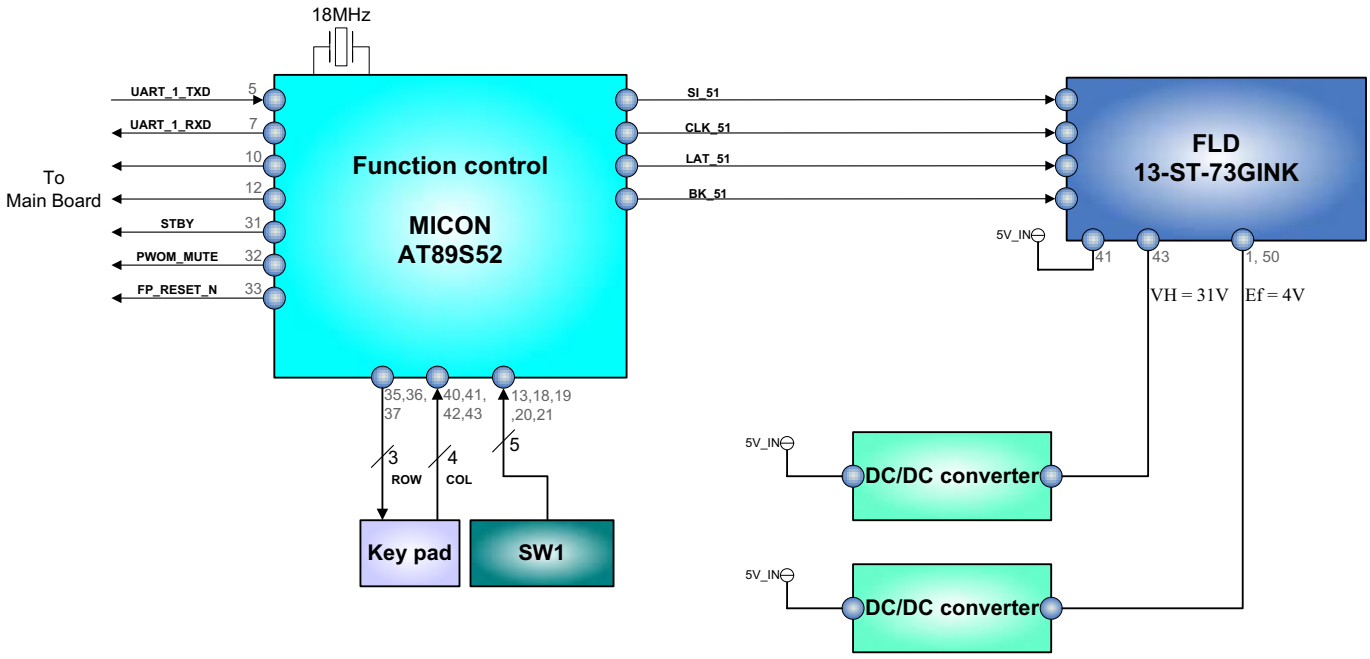
8. NO Work : Flow chart



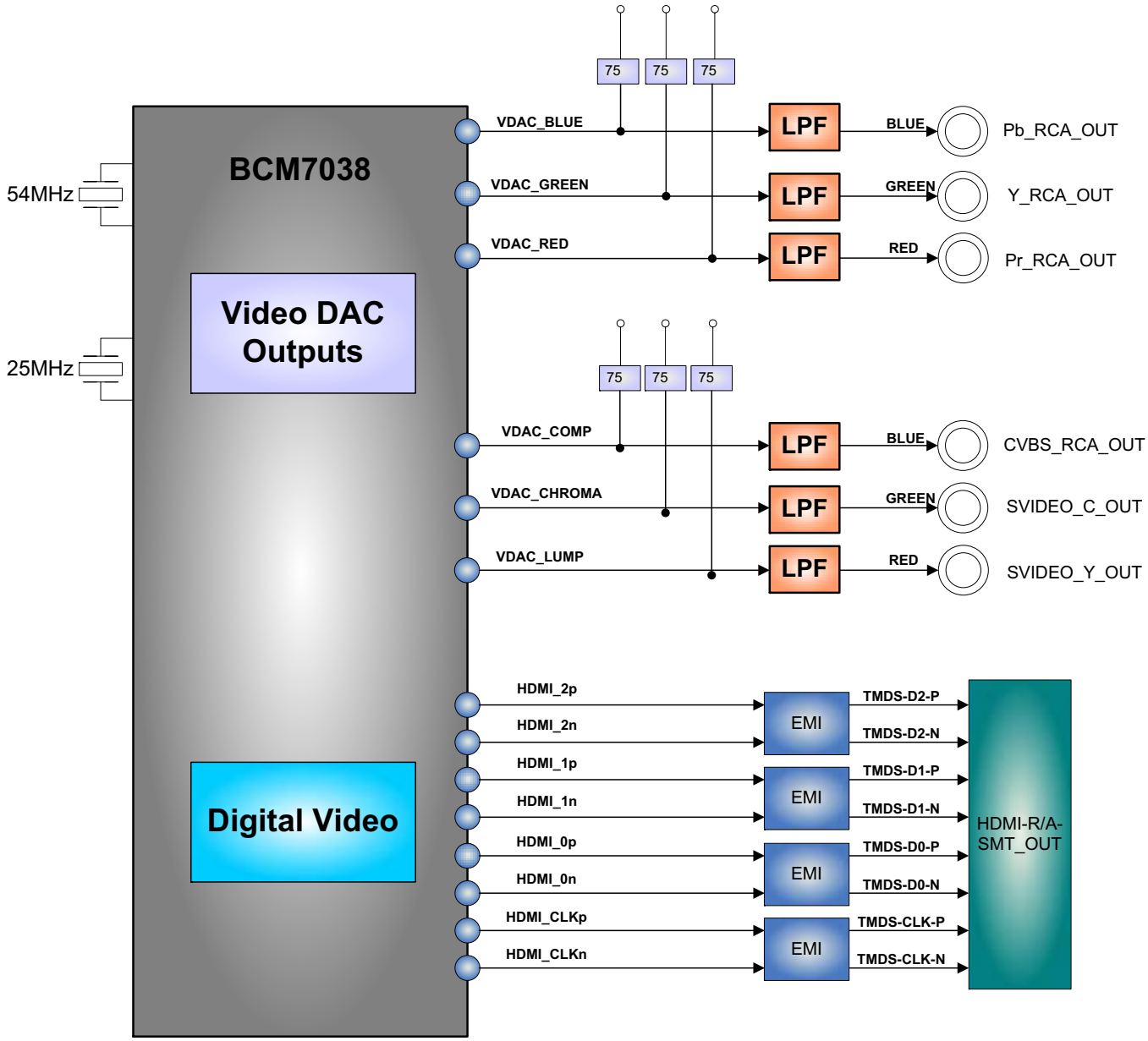
6. Block Diagram & Wiring Diagram



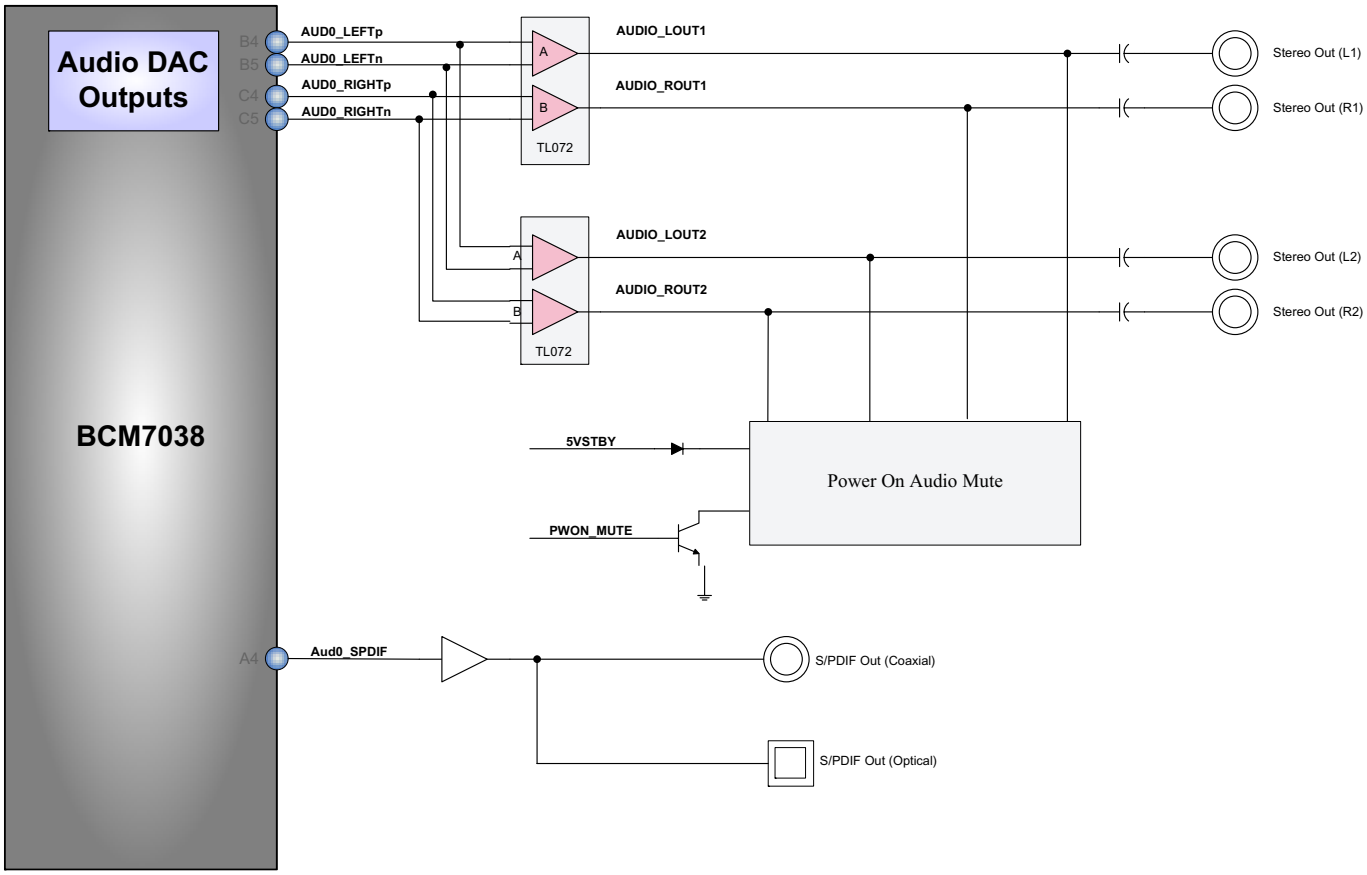
Front Panel


18MHz
UART_1_TXD
5
UART_1_RXD
7
10
12
STBY
31
PWOM_MUTE
32
FP_RESET_N
33
To
Main Board
Function control
MICON
AT89S52
SI_51
CLK_51
LAT_51
BK_51
FLD
13-ST-73GINK
5V_IN
41
43
1, 50
VH = 31V
Ef = 4V
35,36,
37
40,41,
42,43
13,18,19
,20,21
3
ROW
4
COL
5
Key pad
SW1
5V_IN
DC/DC converter
5V_IN
DC/DC converter

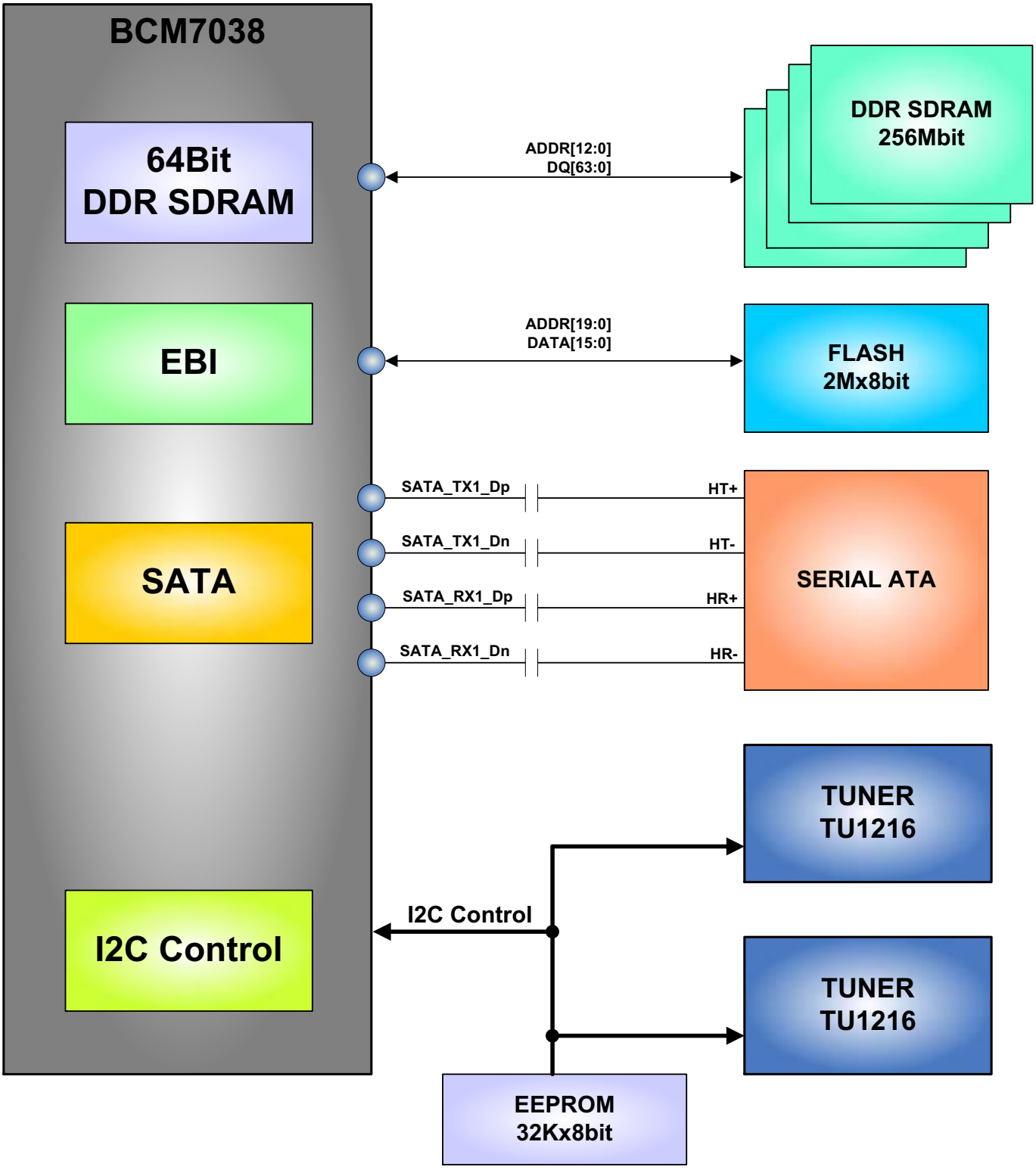
Video Block Diagram

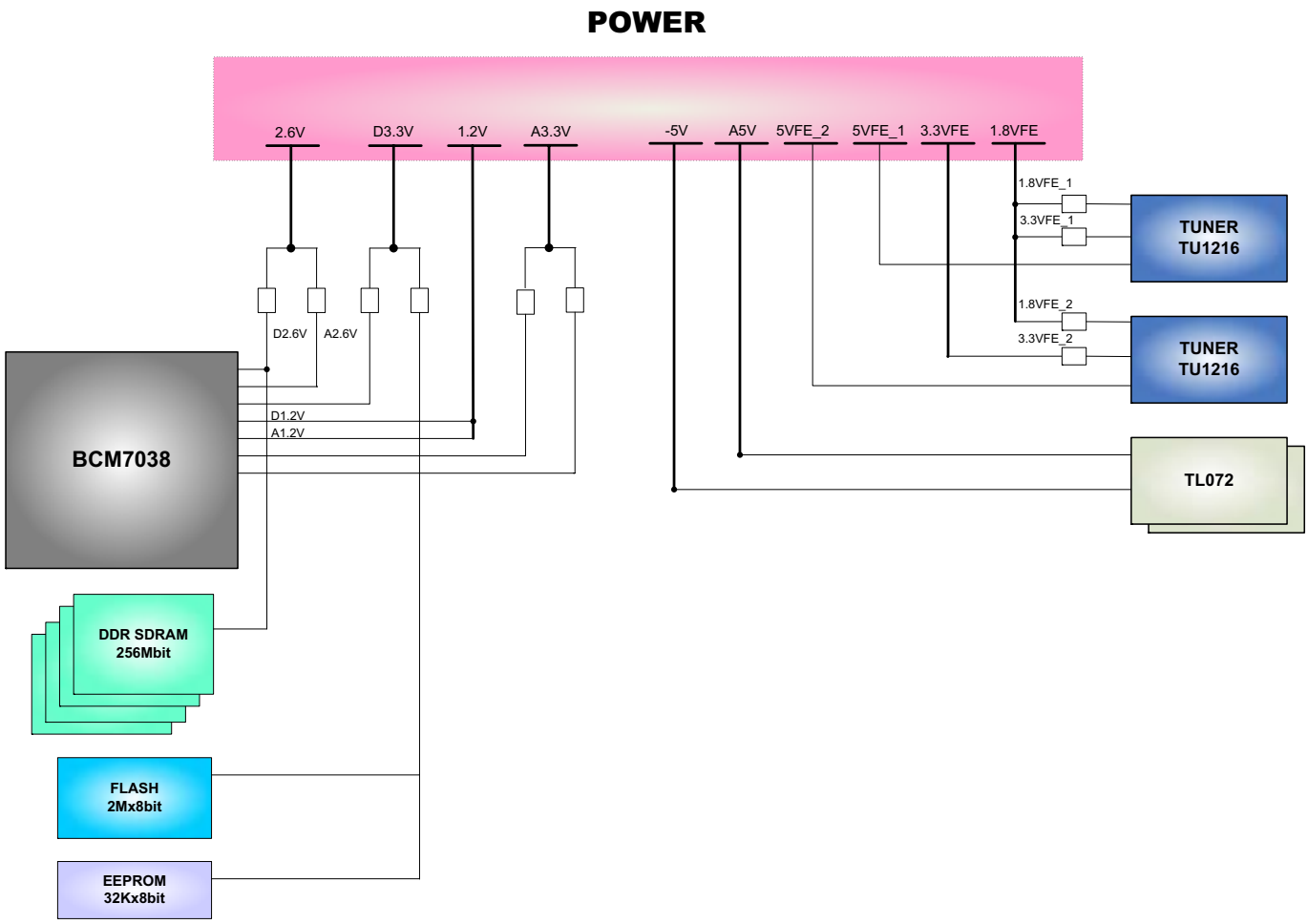


Audio Block Diagram

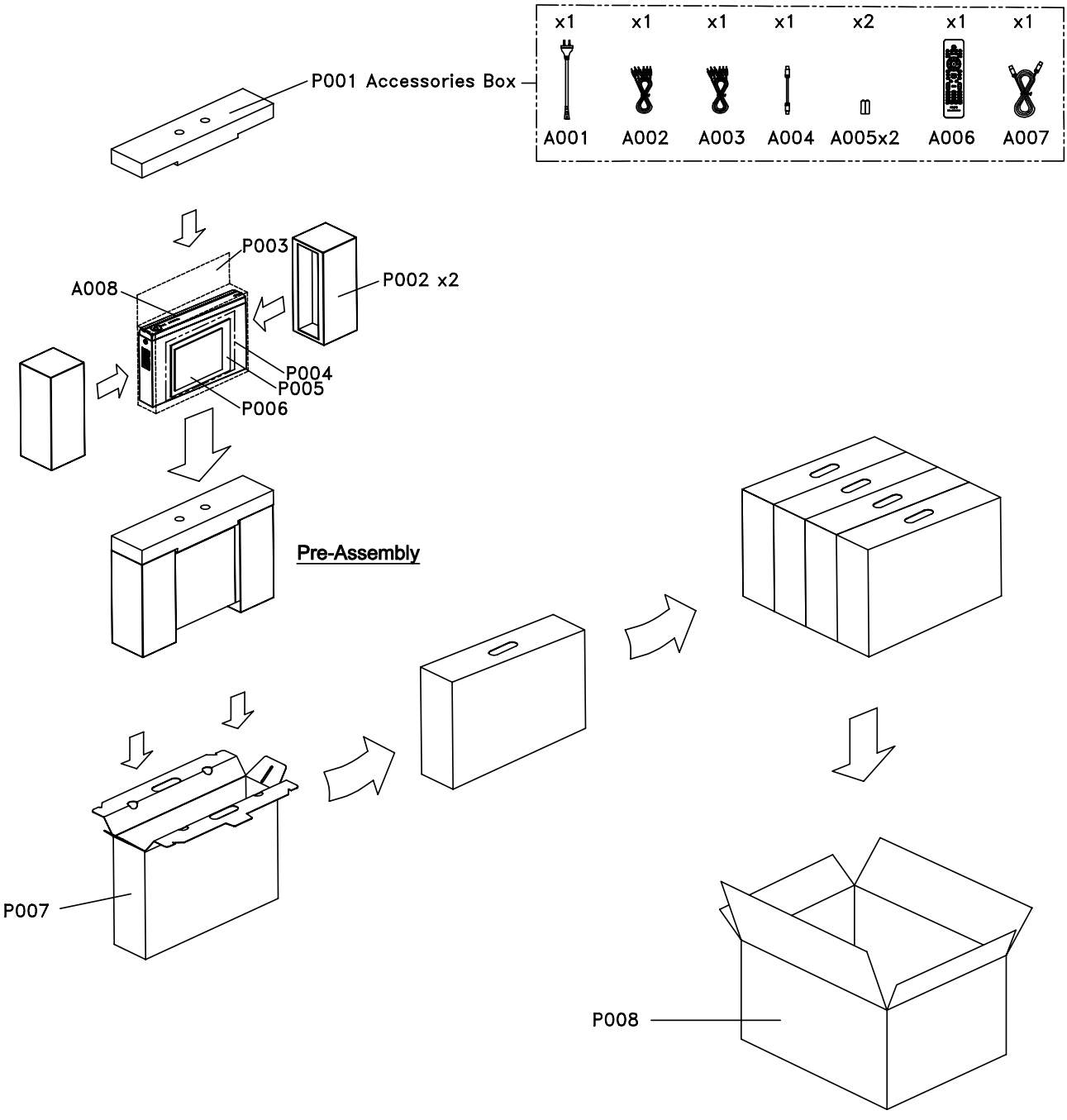


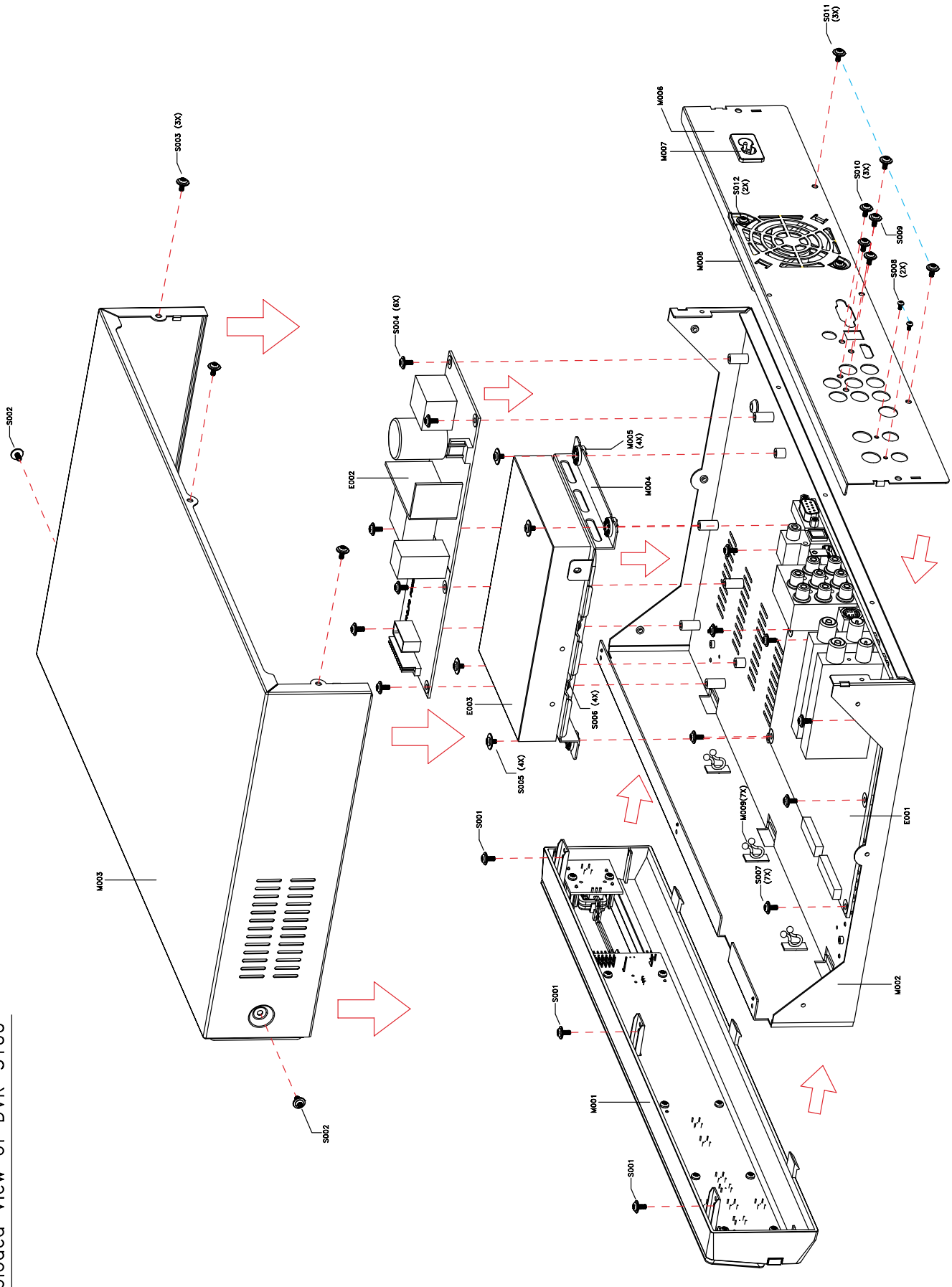
MEMORY/SATA/TUNER




POWER
2.6V
D3.3V
1.2V
A3.3V
-5V
A5V
5VFE_2
5VFE_1
3.3VFE
1.8VFE
1.8VFE_1
3.3VFE_1
TUNER
TU1216
1.8VFE_2
3.3VFE_2
TUNER
TU1216
D2.6V
A2.6V
D1.2V
A1.2V
BCM7038
TL072
DDR SDRAM
256Mbit
FLASH
2Mx8bit
EEPROM
32Kx8bit

7. Mechanical Exploded view & Packaging drawing





Exploded View of DVR-5100

8. Service Parts List & screw list

SERVICE PARTS LIST

A001	996510004493	⚠	POWER CORD
A002	996510004494		AUDIO/VIDEO CINCH CABLE
A003	996510004483		Y-PB-PR CINCH CABLE 150CM
A004	996510004495		RF CABLE 12,5CM (SHORT)
A006	996510004500		REMOTE CONTROL UNIT
A007	996510004496		RF CABLE 100CM (LONG)
C02	996510004497		POWER CABLE 14PIN 46cm
C03	996510004498		SATA POWER CABLE 4 Pin 20cm
C04	996510004499		SATA SIGNAL CABLE 38cm
E001	996510004468		MAIN BOARD PCB-A
E002	996510004481	⚠	POWER SUPPLY BOARD
E003	996510004482		HARD DISK 160G (DVR5100)
E003	996510004532		HARD DISK 250G (DVR7100)
M001	996510004537		FRONT COMPLETE ASSY
M002	996510004485		BOTTOM COVER
M003	996510004484		TOP COVER
M005	996510004488		RUBBER DAMPER, HDD
M006	996510004486		BACK PANEL
M007	996510004489	⚠	MAINS SOCKET + HYBRID WIRE ASSY
M008	996510004487		ELECTICAL FAN 12VDC
M009	996510004490		WIRE CLAMP
S005	996510004491		SCREW M3x6mm w/Washer D=10mm
S006	996510004492		SPECIAL SCREW 6#-32x1/4"
U32	996510004479		TUNER UNIT TU1216L/IVP

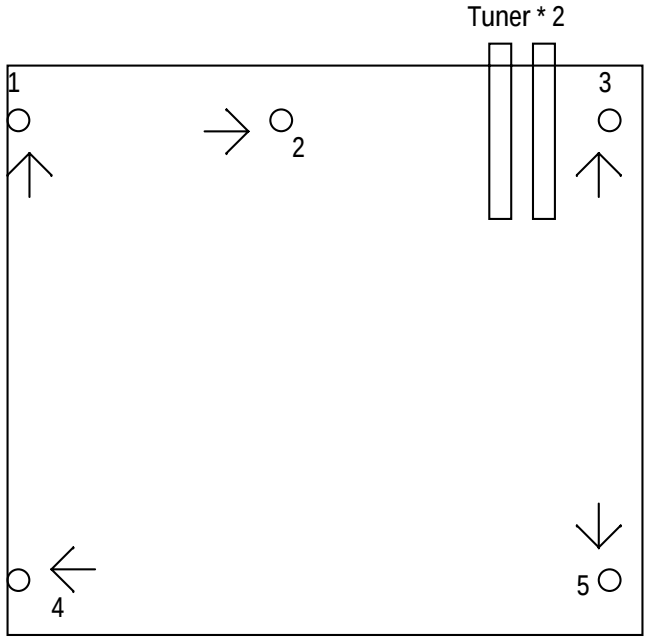
NOTE: ONLY THE PARTS MENTIONED IN THIS LIST ARE NORMAL SERVICE PARTS

SCREW LIST

S001	SCREW D3x6mm
S002	SCREW D3x6mm
S003	SCREW D3x6mm
S004	SCREW M3x6mm
S007	SCREW M3x6mm
S008	SCREW D2x4mm
S009	SCREW M3x6mm
S010	SCREW D3x8mm
S011	SCREW D3x6mm
S012	SCREW D3x8mm

9. Annex Attachments:

- **Pcba drawing & Circuit diagrams**



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TEL:886-3-597-9050 # 559

ZINWELL

Title	Philips_DVR	
Size A	Document Number Note	Rev 1.1
Date: Monday, April 16, 2007	Sheet 1 of 19	

U1-13
BCM7038B0

64Bit DDR SDRAM

SD_ADDR12 AG18 BCM7038_SD_ADDR12
SD_ADDR11 AE18 BCM7038_SD_ADDR11
SD_ADDR10 AG16 BCM7038_SD_ADDR10
SD_ADDR9 AG17 BCM7038_SD_ADDR9
SD_ADDR8 AF18 BCM7038_SD_ADDR8
SD_ADDR7 AJ17 BCM7038_SD_ADDR7
SD_ADDR6 AD17 BCM7038_SD_ADDR6
SD_ADDR5 AH17 BCM7038_SD_ADDR5
SD_ADDR4 AE17 BCM7038_SD_ADDR4
SD_ADDR3 AH16 BCM7038_SD_ADDR3
SD_ADDR2 AE16 BCM7038_SD_ADDR2
SD_ADDR1 AJ16 BCM7038_SD_ADDR1
SD_ADDR0 AF15 BCM7038_SD_ADDR0

SD_BA1 AD15 BCM7038_SD_BA1
SD_BA0 AG15 BCM7038_SD_BA0

SD_CK1 AH10 BCM7038_SD_CK1
SD_CK1 AJ10 BCM7038_SD_CK1b
SD_CK0 AH23 BCM7038_SD_CK0
SD_CK0 AJ23 BCM7038_SD_CK0b
SD_CKE AJ18 BCM7038_SD_CKE
SD_CS0 AH15 BCM7038_SD_CS0b
SD_RAS AE14 BCM7038_SD_RASb
SD_CAS AD14 BCM7038_SD_CASb
SD_WE AJ15 BCM7038_SD_WEb

SD_DQ63 AG5 BCM7038_SD_DQ63
SD_DQ62 AF6 BCM7038_SD_DQ62
SD_DQ61 AF7 BCM7038_SD_DQ61
SD_DQ60 AG7 BCM7038_SD_DQ60
SD_DQ59 AH5 BCM7038_SD_DQ59
SD_DQ58 AJ5 BCM7038_SD_DQ58
SD_DQ57 AJ6 BCM7038_SD_DQ57
SD_DQ56 AH7 BCM7038_SD_DQ56
SD_DQ55 AE8 BCM7038_SD_DQ55
SD_DQ54 AG8 BCM7038_SD_DQ54
SD_DQ53 AF9 BCM7038_SD_DQ53
SD_DQ52 AG9 BCM7038_SD_DQ52
SD_DQ51 AJ7 BCM7038_SD_DQ51
SD_DQ50 AH8 BCM7038_SD_DQ50
SD_DQ49 AH9 BCM7038_SD_DQ49
SD_DQ48 AJ9 BCM7038_SD_DQ48
SD_DQ47 AE10 BCM7038_SD_DQ47
SD_DQ46 AG10 BCM7038_SD_DQ46
SD_DQ45 AF11 BCM7038_SD_DQ45
SD_DQ44 AG11 BCM7038_SD_DQ44
SD_DQ43 AH11 BCM7038_SD_DQ43
SD_DQ42 AJ11 BCM7038_SD_DQ42
SD_DQ41 AJ12 BCM7038_SD_DQ41
SD_DQ40 AH13 BCM7038_SD_DQ40
SD_DQ39 AD12 BCM7038_SD_DQ39
SD_DQ38 AE12 BCM7038_SD_DQ38
SD_DQ37 AD13 BCM7038_SD_DQ37
SD_DQ36 AF13 BCM7038_SD_DQ36
SD_DQ35 AJ13 BCM7038_SD_DQ35
SD_DQ34 AG13 BCM7038_SD_DQ34
SD_DQ33 AJ14 BCM7038_SD_DQ33
SD_DQ32 AG14 BCM7038_SD_DQ32
SD_DQ31 AE19 BCM7038_SD_DQ31
SD_DQ30 AG19 BCM7038_SD_DQ30
SD_DQ29 AF20 BCM7038_SD_DQ29
SD_DQ28 AG20 BCM7038_SD_DQ28
SD_DQ27 AH18 BCM7038_SD_DQ27
SD_DQ26 AH19 BCM7038_SD_DQ26
SD_DQ25 AH20 BCM7038_SD_DQ25
SD_DQ24 AJ20 BCM7038_SD_DQ24
SD_DQ23 AD21 BCM7038_SD_DQ23
SD_DQ22 AE21 BCM7038_SD_DQ22
SD_DQ21 AD22 BCM7038_SD_DQ21
SD_DQ20 AE22 BCM7038_SD_DQ20
SD_DQ19 AH21 BCM7038_SD_DQ19
SD_DQ18 AJ21 BCM7038_SD_DQ18
SD_DQ17 AJ22 BCM7038_SD_DQ17
SD_DQ16 AG23 BCM7038_SD_DQ16
SD_DQ15 AG22 BCM7038_SD_DQ15
SD_DQ14 AE23 BCM7038_SD_DQ14
SD_DQ13 AG24 BCM7038_SD_DQ13
SD_DQ12 AE25 BCM7038_SD_DQ12
SD_DQ11 AJ24 BCM7038_SD_DQ11
SD_DQ10 AH24 BCM7038_SD_DQ10
SD_DQ9 AH25 BCM7038_SD_DQ9
SD_DQ8 AJ26 BCM7038_SD_DQ8
SD_DQ7 AG25 BCM7038_SD_DQ7
SD_DQ6 AF26 BCM7038_SD_DQ6
SD_DQ5 AF27 BCM7038_SD_DQ5
SD_DQ4 AG27 BCM7038_SD_DQ4
SD_DQ3 AH26 BCM7038_SD_DQ3
SD_DQ2 AJ27 BCM7038_SD_DQ2
SD_DQ1 AJ28 BCM7038_SD_DQ1
SD_DQ0 AH28 BCM7038_SD_DQ0

SD_DQS7 AH6 BCM7038_SD_DQS7
SD_DQS6 AJ8 BCM7038_SD_DQS6
SD_DQS5 AH12 BCM7038_SD_DQS5
SD_DQS4 AH14 BCM7038_SD_DQS4
SD_DQS3 AJ19 BCM7038_SD_DQS3
SD_DQS2 AH22 BCM7038_SD_DQS2
SD_DQS1 AJ25 BCM7038_SD_DQS1
SD_DQS0 AH27 BCM7038_SD_DQS0

SD_DQM7 AG6 BCM7038_SD_DQM7
SD_DQM6 AD10 BCM7038_SD_DQM6
SD_DQM5 AD11 BCM7038_SD_DQM5
SD_DQM4 AG12 BCM7038_SD_DQM4
SD_DQM3 AD20 BCM7038_SD_DQM3
SD_DQM2 AG21 BCM7038_SD_DQM2
SD_DQM1 AF24 BCM7038_SD_DQM1
SD_DQM0 AG26 BCM7038_SD_DQM0

SD_VREF AJ4
SD_VREF AJ29

DDR_VREF1
DDR_VREF2
C36 470pF
C35 1uF
R15 4.99K (DNI) 1%
R21 4.99K (DNI) 1%
C38 1uF
C37 470pF

"Route VREF with 30-mil trace and CAP must be nearly at 7038".

RN1: BCM7038_SD_CKE, BCM7038_SD_ADDR12, BCM7038_SD_ADDR9, BCM7038_SD_ADDR7 → DDR_CKE, DDR_ADDR12, DDR_ADDR9, DDR_ADDR7
RN4: BCM7038_SD_ADDR5, BCM7038_SD_ADDR3, BCM7038_SD_ADDR1, BCM7038_SD_ADDR10 → DDR_ADDR5, DDR_ADDR3, DDR_ADDR1, DDR_ADDR10
RN7: BCM7038_SD_BA0, BCM7038_SD_WEb, BCM7038_SD_CS0b → DDR_BA0, DDR_WEb, DDR_CS0b
RN10: BCM7038_SD_ADDR11, BCM7038_SD_ADDR8, BCM7038_SD_ADDR6, BCM7038_SD_ADDR4 → DDR_ADDR11, DDR_ADDR8, DDR_ADDR6, DDR_ADDR4
RN15: BCM7038_SD_ADDR2, BCM7038_SD_ADDR0, BCM7038_SD_BA1, BCM7038_SD_RASb → DDR_ADDR2, DDR_ADDR0, DDR_BA1, DDR_RASb
BCM7038_SD_CASb — R1 22 — DDR_CASb

Route clocks as differential pairs

BCM7038_SD_CK1 — R2 22 — DDR_CK1
BCM7038_SD_CK1b — R3 22 — DDR_CK1b
BCM7038_SD_CK0 — R4 22 — DDR_CK0
BCM7038_SD_CK0b — R5 22 — DDR_CK0b

DDR_VTT

RN2: BCM7038_SD_DQ0, BCM7038_SD_DQ1, BCM7038_SD_DQS0, BCM7038_SD_DQ2 → DDR_DQ0, DDR_DQ1, DDR_DQS0, DDR_DQ2
RN3: 62 — DDR_VTT
RN5: BCM7038_SD_DQ3, BCM7038_SD_DQ8, BCM7038_SD_DQ9 → DDR_DQ3, DDR_DQ8, DDR_DQ9
RN6: 62
RN8: BCM7038_SD_DQS1, BCM7038_SD_DQ10, BCM7038_SD_DQ11 → DDR_DQS1, DDR_DQ10, DDR_DQ11
RN9: 62
RN11: BCM7038_SD_DQ16, BCM7038_SD_DQ17, BCM7038_SD_DQS2, BCM7038_SD_DQ18 → DDR_DQ16, DDR_DQ17, DDR_DQS2, DDR_DQ18
RN12: 62
RN13: BCM7038_SD_DQ19, BCM7038_SD_DQ24, BCM7038_SD_DQ25 → DDR_DQ19, DDR_DQ24, DDR_DQ25
RN14: 62
RN16: BCM7038_SD_DQS3, BCM7038_SD_DQ26, BCM7038_SD_DQ27 → DDR_DQS3, DDR_DQ26, DDR_DQ27
RN17: 62
RN18: BCM7038_SD_DQ32, BCM7038_SD_DQ33, BCM7038_SD_DQS4, BCM7038_SD_DQ34 → DDR_DQ32, DDR_DQ33, DDR_DQS4, DDR_DQ34
RN19: 62
BCM7038_SD_DQ35 — R6 22 — DDR_DQ35; R7 62
BCM7038_SD_DQ40 — R8 22 — DDR_DQ40; R9 62
RN20: BCM7038_SD_DQ41, BCM7038_SD_DQS5, BCM7038_SD_DQ42, BCM7038_SD_DQ43 → DDR_DQ41, DDR_DQS5, DDR_DQ42, DDR_DQ43
RN21: 62
RN22: BCM7038_SD_DQ48, BCM7038_SD_DQ49, BCM7038_SD_DQS6, BCM7038_SD_DQ50 → DDR_DQ48, DDR_DQ49, DDR_DQS6, DDR_DQ50
RN23: 62
RN24: BCM7038_SD_DQ51, BCM7038_SD_DQ56, BCM7038_SD_DQ57 → DDR_DQ51, DDR_DQ56, DDR_DQ57
RN25: 62
RN26: BCM7038_SD_DQS7, BCM7038_SD_DQ58, BCM7038_SD_DQ59 → DDR_DQS7, DDR_DQ58, DDR_DQ59
RN27: 62
RN28: BCM7038_SD_DQ4, BCM7038_SD_DQ5, BCM7038_SD_DQM0, BCM7038_SD_DQ6 → DDR_DQ4, DDR_DQ5, DDR_DQM0, DDR_DQ6
RN29: 62
BCM7038_SD_DQ7 — R10 22 — DDR_DQ7; R11 62
RN30: BCM7038_SD_DQ12, BCM7038_SD_DQ13, BCM7038_SD_DQM1, BCM7038_SD_DQ14 → DDR_DQ12, DDR_DQ13, DDR_DQM1, DDR_DQ14
RN31: 62
RN32: BCM7038_SD_DQ15, BCM7038_SD_DQ20, BCM7038_SD_DQ21 → DDR_DQ15, DDR_DQ20, DDR_DQ21
RN33: 62
RN34: BCM7038_SD_DQM2, BCM7038_SD_DQ22, BCM7038_SD_DQ23 → DDR_DQM2, DDR_DQ22, DDR_DQ23
RN35: 62
RN36: BCM7038_SD_DQ28, BCM7038_SD_DQ29, BCM7038_SD_DQM3, BCM7038_SD_DQ30 → DDR_DQ28, DDR_DQ29, DDR_DQM3, DDR_DQ30
RN37: 62
BCM7038_SD_DQ31 — R12 22 — DDR_DQ31; R13 62
RN38: BCM7038_SD_DQ36, BCM7038_SD_DQ37, BCM7038_SD_DQM4, BCM7038_SD_DQ38 → DDR_DQ36, DDR_DQ37, DDR_DQM4, DDR_DQ38
RN39: 62
RN40: BCM7038_SD_DQ39, BCM7038_SD_DQ44, BCM7038_SD_DQ45 → DDR_DQ39, DDR_DQ44, DDR_DQ45
RN41: 62
RN42: BCM7038_SD_DQM5, BCM7038_SD_DQ46, BCM7038_SD_DQ47 → DDR_DQM5, DDR_DQ46, DDR_DQ47
RN43: 62
RN44: BCM7038_SD_DQ52, BCM7038_SD_DQ53, BCM7038_SD_DQM6, BCM7038_SD_DQ54 → DDR_DQ52, DDR_DQ53, DDR_DQM6, DDR_DQ54
RN45: 62
BCM7038_SD_DQ55 — R17 22 — DDR_DQ55; R18 62
BCM7038_SD_DQ60 — R19 22 — DDR_DQ60; R20 62
RN46: BCM7038_SD_DQ61, BCM7038_SD_DQM7, BCM7038_SD_DQ62, BCM7038_SD_DQ63 → DDR_DQ61, DDR_DQM7, DDR_DQ62, DDR_DQ63
RN47: 62

3 DDR_DQ[63:0]
3 DDR_ADDR[12:0]
3 DDR_DQS0 … DDR_DQS7
3 DDR_DQM0 … DDR_DQM7
3 DDR_BA1, DDR_BA0, DDR_CKE, DDR_CS0b, DDR_RASb, DDR_CASb, DDR_WEb
3 DDR_CK0, DDR_CK0b, DDR_CK1, DDR_CK1b

D2.6V_BCM7038
BC1 0.1uF
BC2 0.1uF

DDR_VTT
C311 NI 0805
C312 NI 0805
C313 NI 0805
C314 NI 0805
C315 NI 0805
C316 NI 0805

DDR_VTT
C1 0.1uF
C2 0.01uF
C3 0.1uF
C4 0.01uF
C5 0.1uF
C6 0.01uF
C7 0.1uF
C8 0.01uF
C9 0.1uF
C10 0.01uF
C11 0.1uF
C12 0.01uF
C13 0.1uF
C14 0.01uF
C15 1000pF
C16 0.01uF
C17 4.7uF
C18 0.01uF
C19 1000pF
C20 0.01uF
C21 1000pF
C22 0.01uF
C23 1000pF
C24 0.01uF
C25 1000pF
C26 0.01uF
C27 1000pF
C28 470pF
C29 470pF
C30 470pF
C31 470pF
C32 470pF
C33 470pF
C34 470pF

New DDR routing rules:

All timing is relative the CLK/CLKb that arrive at the destination DDR SDRAM chip.

1) X = CLK/CLKb should be a matched differential pair with a length < 4"

2) Address and control should be X +/- 0.75" (or 100 ps)
3) DQS and DQM should be X +/- 0.75" (or 100 ps)
4) All DQs should match corresponding byte lane DQS/DQMs within +/- 0.20" (or 30 ps)

5) Place 22 ohm resisters on this page near BCM7038.

6) Place 62 ohm resisters for DQ signals midpoint between BCM7038 and DDR SDRAM

7) Place DDR_VREF1/2 resistor dividers near BCM7038

8) Trace impedances need to be 60 ohms +/- 10% (54-66 ohms)

9) Route VREF with 30-mil trace and at least 1 high quality ceramic bypass capacitor for each connection to a device.

10) All traces should have a >= 3 to 1 spacing ratio fom the reference GND/PWR layer. (e.g. 15 mil line-to-line spacing for a 5 mil dielectric thickness)

02

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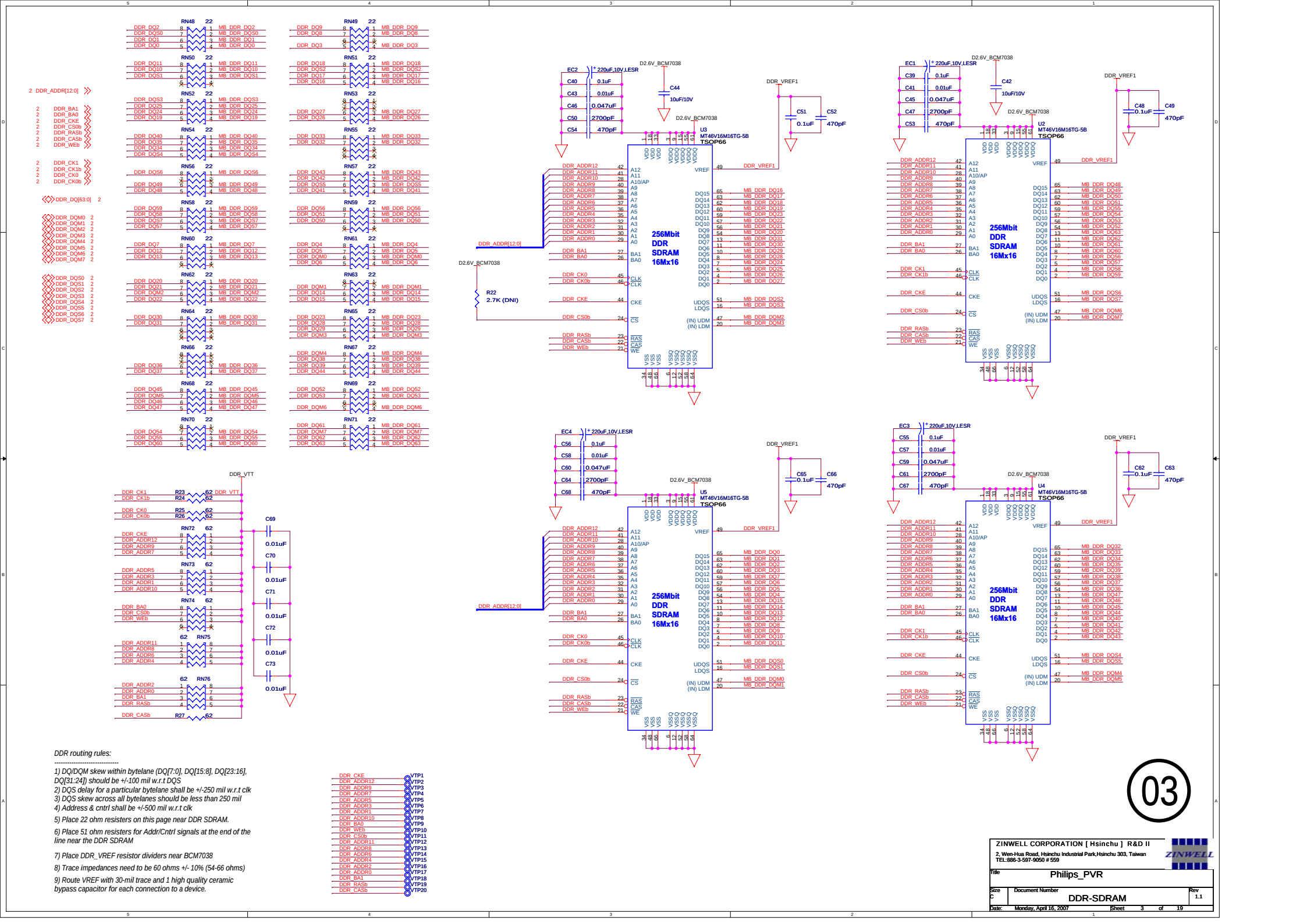
Title: Philips_DVR
Size: C
Document Number: DDR TERM/CONN
Rev: 1.1
Date: Monday, April 16, 2007
Sheet 2 of 19


RN48 22
DDR_DQ2 MB_DDR_DQ2
DDR_DQS0 MB_DDR_DQS0
DDR_DQ1 MB_DDR_DQ1
DDR_DQ0 MB_DDR_DQ0
RN49 22
DDR_DQ9 MB_DDR_DQ9
DDR_DQ8 MB_DDR_DQ8
DDR_DQ3 MB_DDR_DQ3
RN50 22
DDR_DQ11 MB_DDR_DQ11
DDR_DQ10 MB_DDR_DQ10
DDR_DQS1 MB_DDR_DQS1
RN51 22
DDR_DQ18 MB_DDR_DQ18
DDR_DQS2 MB_DDR_DQS2
DDR_DQ17 MB_DDR_DQ17
DDR_DQ16 MB_DDR_DQ16
RN52 22
DDR_DQS3 MB_DDR_DQS3
DDR_DQ25 MB_DDR_DQ25
DDR_DQ24 MB_DDR_DQ24
DDR_DQ19 MB_DDR_DQ19
RN53 22
DDR_DQ27 MB_DDR_DQ27
DDR_DQ26 MB_DDR_DQ26
RN54 22
DDR_DQ40 MB_DDR_DQ40
DDR_DQ35 MB_DDR_DQ35
DDR_DQ34 MB_DDR_DQ34
DDR_DQS4 MB_DDR_DQS4
RN55 22
DDR_DQ33 MB_DDR_DQ33
DDR_DQ32 MB_DDR_DQ32
RN56 22
DDR_DQS6 MB_DDR_DQS6
DDR_DQ49 MB_DDR_DQ49
DDR_DQ48 MB_DDR_DQ48
RN57 22
DDR_DQ43 MB_DDR_DQ43
DDR_DQ42 MB_DDR_DQ42
DDR_DQS5 MB_DDR_DQS5
DDR_DQ41 MB_DDR_DQ41
RN58 22
DDR_DQ59 MB_DDR_DQ59
DDR_DQ58 MB_DDR_DQ58
DDR_DQS7 MB_DDR_DQS7
DDR_DQ57 MB_DDR_DQ57
RN59 22
DDR_DQ56 MB_DDR_DQ56
DDR_DQ51 MB_DDR_DQ51
DDR_DQ50 MB_DDR_DQ50
RN60 22
DDR_DQ7 MB_DDR_DQ7
DDR_DQ12 MB_DDR_DQ12
DDR_DQ13 MB_DDR_DQ13
RN61 22
DDR_DQ4 MB_DDR_DQ4
DDR_DQ5 MB_DDR_DQ5
DDR_DQM0 MB_DDR_DQM0
DDR_DQ6 MB_DDR_DQ6
RN62 22
DDR_DQ20 MB_DDR_DQ20
DDR_DQ21 MB_DDR_DQ21
DDR_DQM2 MB_DDR_DQM2
DDR_DQ22 MB_DDR_DQ22
RN63 22
DDR_DQM1 MB_DDR_DQM1
DDR_DQ14 MB_DDR_DQ14
DDR_DQ15 MB_DDR_DQ15
RN64 22
DDR_DQ30 MB_DDR_DQ30
DDR_DQ31 MB_DDR_DQ31
RN65 22
DDR_DQ23 MB_DDR_DQ23
DDR_DQ28 MB_DDR_DQ28
DDR_DQ29 MB_DDR_DQ29
DDR_DQM3 MB_DDR_DQM3
RN66 22
DDR_DQ36 MB_DDR_DQ36
DDR_DQ37 MB_DDR_DQ37
RN67 22
DDR_DQM4 MB_DDR_DQM4
DDR_DQ38 MB_DDR_DQ38
DDR_DQ39 MB_DDR_DQ39
DDR_DQ44 MB_DDR_DQ44
RN68 22
DDR_DQ45 MB_DDR_DQ45
DDR_DQM5 MB_DDR_DQM5
DDR_DQ46 MB_DDR_DQ46
DDR_DQ47 MB_DDR_DQ47
RN69 22
DDR_DQ52 MB_DDR_DQ52
DDR_DQ53 MB_DDR_DQ53
DDR_DQM6 MB_DDR_DQM6
RN70 22
DDR_DQ54 MB_DDR_DQ54
DDR_DQ55 MB_DDR_DQ55
DDR_DQ60 MB_DDR_DQ60
RN71 22
DDR_DQ61 MB_DDR_DQ61
DDR_DQM7 MB_DDR_DQM7
DDR_DQ62 MB_DDR_DQ62
DDR_DQ63 MB_DDR_DQ63
2 DDR_ADDR[12:0]
2 DDR_BA1
2 DDR_BA0
2 DDR_CKE
2 DDR_CS0b
2 DDR_RASb
2 DDR_CASb
2 DDR_WEb
2 DDR_CK1
2 DDR_CK1b
2 DDR_CK0
2 DDR_CK0b
DDR_DQ[63:0] 2
DDR_DQM0 2
DDR_DQM1 2
DDR_DQM2 2
DDR_DQM3 2
DDR_DQM4 2
DDR_DQM5 2
DDR_DQM6 2
DDR_DQM7 2
DDR_DQS0 2
DDR_DQS1 2
DDR_DQS2 2
DDR_DQS3 2
DDR_DQS4 2
DDR_DQS5 2
DDR_DQS6 2
DDR_DQS7 2
D2.6V_BCM7038
EC2 220uF,10V,LESR
C40 0.1uF
C43 0.01uF
C46 0.047uF
C50 2700pF
C54 470pF
C44 10uF/10V
C51 0.1uF
C52 470pF
DDR_VREF1
U3 MT46V16M16TG-5B TSOP66
256Mbit DDR SDRAM 16Mx16
DDR_ADDR[12:0]
R22 2.7K (DNI)
EC1 220uF,10V,LESR
C39 0.1uF
C41 0.01uF
C45 0.047uF
C47 2700pF
C53 470pF
C42 10uF/10V
C48 0.1uF
C49 470pF
U2 MT46V16M16TG-5B TSOP66
EC4 220uF,10V,LESR
C56 0.1uF
C58 0.01uF
C60 0.047uF
C64 2700pF
C68 470pF
C65 0.1uF
C66 470pF
U5 MT46V16M16TG-5B TSOP66
EC3 220uF,10V,LESR
C55 0.1uF
C57 0.01uF
C59 0.047uF
C61 2700pF
C67 470pF
C62 0.1uF
C63 470pF
U4 MT46V16M16TG-5B TSOP66
DDR_VTT
R23 62 DDR_VTT
R24 62
R25 62
R26 62
R27 62
C69 0.01uF
C70 0.01uF
C71 0.01uF
C72 0.01uF
C73 0.01uF
RN72 62
RN73 62
RN74 62
RN75 62
RN76 62
DDR routing rules:
1) DQ/DQM skew within bytelane (DQ[7:0], DQ[15:8], DQ[23:16], DQ[31:24]) should be +/-100 mil w.r.t DQS
2) DQS delay for a particular bytelane shall be +/-250 mil w.r.t clk
3) DQS skew across all bytelanes should be less than 250 mil
4) Address & cntrl shall be +/-500 mil w.r.t clk
5) Place 22 ohm resisters on this page near DDR SDRAM.
6) Place 51 ohm resisters for Addr/Cntrl signals at the end of the line near the DDR SDRAM
7) Place DDR_VREF resistor dividers near BCM7038
8) Trace impedances need to be 60 ohms +/- 10% (54-66 ohms)
9) Route VREF with 30-mil trace and 1 high quality ceramic bypass capacitor for each connection to a device.
VTP1 VTP2 VTP3 VTP4 VTP5 VTP6 VTP7 VTP8 VTP9 VTP10 VTP11 VTP12 VTP13 VTP14 VTP15 VTP16 VTP17 VTP18 VTP19 VTP20
03
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TEL:886-3-597-9050 # 559
ZINWELL
Title
Philips_PVR
Size C
Document Number
DDR-SDRAM
Rev 1.1
Date: Monday, April 16, 2007
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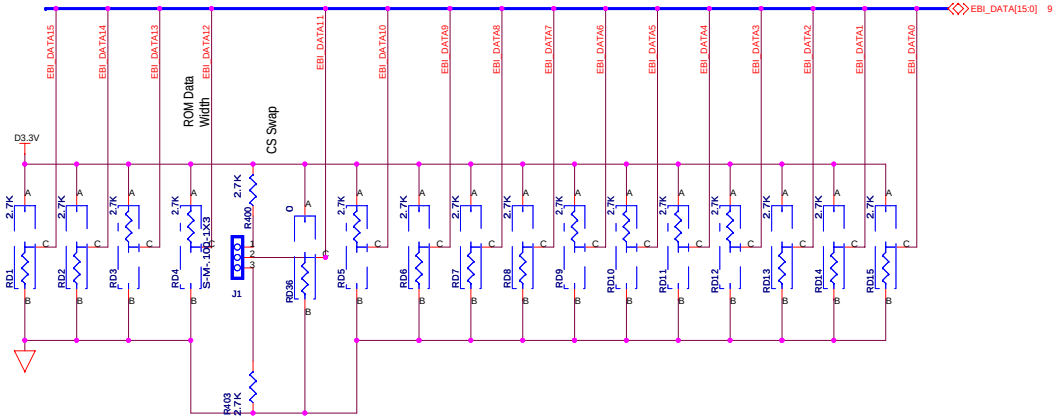
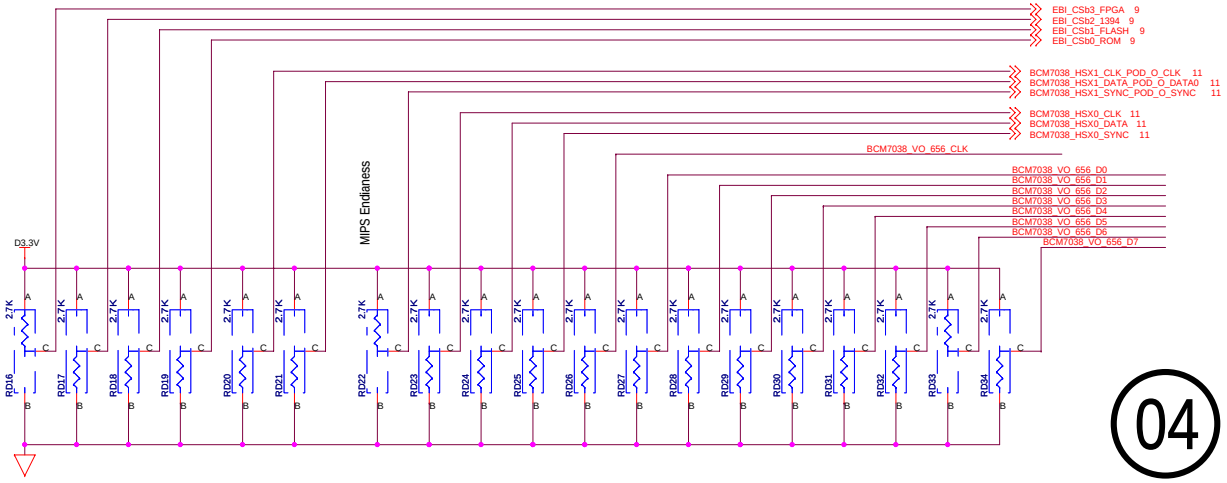
U1-3
BCM7038B0

CCIR656 Video I/O

L29	DVO_21/VI_656_D0	DVO_12/VO_656_D0	N28	BCM7038_VO_656_D0
M25	DVO_22/VI_656_D1	DVO_13/VO_656_D1	N29	BCM7038_VO_656_D1
M26	DVO_23/VI_656_D2	DVO_14/VO_656_D2	P25	BCM7038_VO_656_D2
M27	VI_656_D3	DVO_15/VO_656_D3	P26	BCM7038_VO_656_D3
M28	VI_656_D4	DVO_16/VO_656_D4	P27	BCM7038_VO_656_D4
M29	VI_656_D5	DVO_17/VO_656_D5	P28	BCM7038_VO_656_D5
N25	VI_656_D6	DVO_18/VO_656_D6	P29	BCM7038_VO_656_D6
N26	VI_656_D7	DVO_19/VO_656_D7	R25	BCM7038_VO_656_D7
N27	VI_656_CLK	DVO_20/VO_656_CLK	R26	BCM7038_VO_656_CLK

Strap Bit	Description	Pin	Default	Comments
strap_bypass_cpu_clk	0: Use internal 297 MHz clock 1: Use external CPU clock	EBI_DATA08	0	Run CPU at 297 MHz
strap_crit_word_seq	0: Use sequential addressing 1: Use sub-block addressing	EBI_DATA00	0	Default to sequential addressing though OS may need this changed
strap_ddr_config_1, (MSB) strap_ddr_config_0	0: Reserved 1: 8Mx16 bit parts 2: 16Mx16 bit parts 3: 32Mx16 bit parts	EBI_CS3b, EBI_CS2b	10	Per memory configuration
strap_ddr_config_2	0: 64-bit DDR mode 1: 32-bit DDR mode	HS_CLK1	0	Usually in 64-bit mode
strap_ddr_ext_clock	0: Use internal DDR PLL 1: Use external DDR clock	HS_DATA1	0	Run internal 187 MHz clock
strap_ebi_big_endian	0: EBI system is LITTLE endian 1: EBI system is BIG endian	EBI_DATA10	0	Per system configuration
strap_ebi_boot_memory	0: Boot memory is 8-bit ROM 1: Boot memory is 16-bit ROM	EBI_DATA12	0	Per system configuration
strap_ebi_burst_read_en	0: Disable EBI burst read 1: Enable EBI burst read	EBI_DATA01	0	Usually disabled
strap_ebi_clock_rate	0: Select 54 MHz for EBI clock 1: Select 27 MHz for EBI clock	EBI_DATA13	1	Per system configuration
strap_ebi_cs_swap	0: No swap 1: Swap CS_0 and CS_1 signals	EBI_DATA11	0	Per system configuration
strap_ebi_mux_addr_data	0: Don't multiplex EBI address and data 1: Multiplex EBI address and data	EBI_DATA14	0	Usually in non-multiplex mode
strap_ebi_rom_size1, (MSB) strap_ebi_rom_size0	0: 32 Mbyte ROM 1: 16 Mbyte ROM 2: 8 Mbyte ROM 3: 4 Mbyte ROM	EBI_DATA07, EBI_DATA09	0	Per system configuration
strap_ebi_slave	0: EBI is in master mode 1: EBI is in slave mode	VO0_656_1	0	Usually in master mode
strap_ebi_zero_addr	0: Do not zero EBI address 1: Zero upper bits of EBI address	EBI_DATA02	0	Usually a don't care - set to do not zero
strap_mclk_delay_3,(MSB) strap_mclk_delay_2, strap_mclk_delay_1, strap_mclk_delay_0		VO0_656_0, HS_DATA0, HS_SYNC0, HS_CLK0	0000	TBD
strap_pci_client	0: PCI in bridge (master) mode 1: PCI in client (slave) mode	VO0_656_2	0	Usually in master mode
strap_pci_gisbwin_size_1, strap_pci_gisbwin_size_0	0: 32 Mbyte Window 1: 64 Mbyte Window 2: 128 Mbyte Window 3: 256 Mbyte Window	VO0_656_CLK, VO0_656_7	00	Per memory configuration
strap_pci_memwin_size_1, strap_pci_memwin_size_0	0: 32 Mbyte Window 1: 64 Mbyte Window 2: 128 Mbyte Window 3: 256 Mbyte Window	VO0_656_6, VO0_656_5	0000	Per memory configuration
strap_pci_memwin1_en	0: Disable PCI memory window 1 1: Enable PCI memory window 1	VO0_656_3	0	Per system configuration
strap_pci_memwin2_en	0: Disable PCI memory window 2 1: Enable PCI memory window 2	VO0_656_4	0	Per system configuration
strap_spi_slave_enable	0: BSC slave port configured 1: SPI slave port configured	EBI_DATA15	0	Per system configuration - usually in BSC slave
strap_system_big_endian	0: System is LITTLE endian 1: System is BIG endian	HS_SYNC1	0	Per system configuration
strap_xtal_adj_3, (MSB) strap_xtal_adj_2, strap_xtal_adj_1, strap_xtal_adj_0	Adjust the 54 MHz oscillator bias current. Default is 0.	EBI_DATA06, EBI_DATA05, EBI_DATA04, EBI_DATA03	1111	Given existing Tank Circuit
strap_rsvd_0	Reserved	EBI_CS0b	0	Default to 0
strap_rsvd_1	Reserved	EBI_CS1b	0	Default to 0





04

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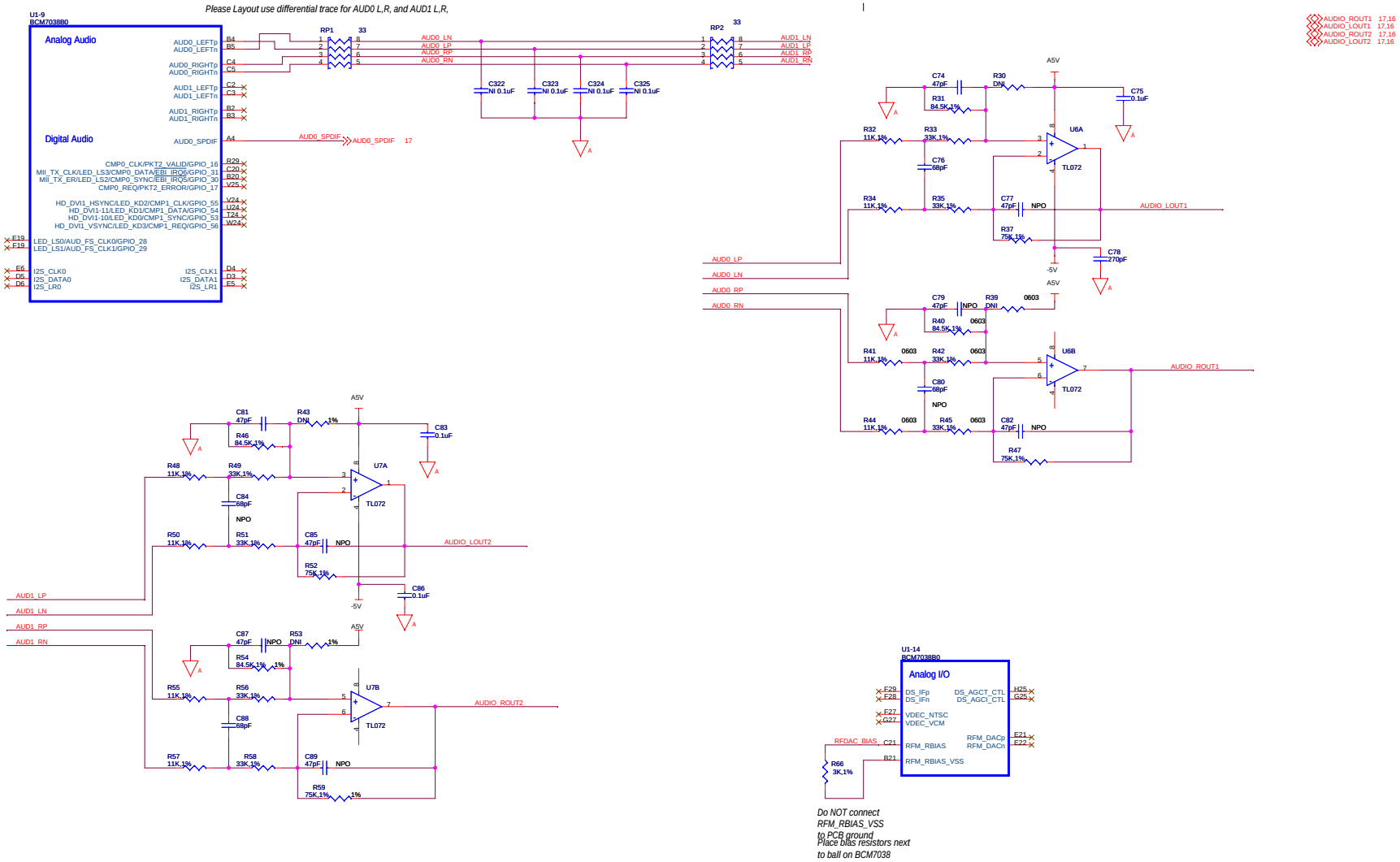
Title	Philips-DVR	
Size C	Document Number CCIR656 , PIN_STRAPOPTION	Rev 1.1
Date: Monday, April 16, 2007	Sheet 4 of 19	



05

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TEL:886-3-597-9050 # 559

Title	Philips_DVR	
Size A2	Document Number: Audio IN/OUT Buffer	Rev 1.1
Date: Monday, April 16, 2007	Sheet 5 of 19	

PLACE NEAR THE BUFFER

VSYNC1 & HSYNC1 Swap

VSYNC1 R79 33 DVI_CTRL_CLK 7,10
HSYNC1 R80 33 DVI_CTRL_DATA 7,10

VDAC_AVDD33

C96 0.1uF C97 0.1uF C98 4.7uF0805

Route VDAC_AVDD33 as a wide trace or fill area on the top layer of the PCB all the way to the connector

Place bias resisters near BCM7038 and try to shield them by GND.

U1-4 BCM7038B0

Video DAC Outputs

R74 562,1% C18 VDAC1_RGB_RBIAS
R75 562,1% C17 VDAC0_CLC_RBIAS

IR3_IN/HSYNC0/GPIO_45 D23
LED_LD0/VSYNC0/GPIO_46 C24
VDAC1_BLUE/Pb C19
VDAC1_GREEN/Y D18
VDAC1_RED/Pr E18
BSC_M3_SCL/HSYNC1/SGPIO_00 F25 HSYNC1
BSC_M3_SDA/VSYNC1/SGPIO_01 E25 VSYNC1
VDAC0_LUMA D16
VDAC0_CHROMA E16
VDAC0_COMPOSITE E17

Video ADC Inputs

SD_Y F24
SD_Pr G24
SD_Pb H24
SD_Chroma K24
SD_Luma J24
SD_CMode R24

Place 75 ohm terminations near BCM7038

VDAC_AVDD33

R68 75,1% R69 75,1% R70 75,1% R71 75,1% R72 75,1% R73 75,1% EC6 1000uF,6.3V,LESR C480 0.1uF

VDAC_BLUE

C420 15pF L55 620nH C423 33pF C424 56pF
C421 8.2pF L56 0.82uH C425 56pF
C422 47pF L57 220nH C426 3.3pF

R390 0 EC60 1000uF Y/G

Place ESD5~7 as close as possible to J19

ESD5 ***PESD0603-060

Place inductors so that the fields from adjacent filters DO NOT couple.

VDAC_GREEN

C441 15pF L1 620nH C430 33pF C431 56pF
C428 8.2pF L2 0.82uH C432 56pF
C429 47pF L3 220nH C433 3.3pF

R391 0 EC61 1000uF Y/G

Place ESD5~7 as close as possible to J19

ESD6 ***PESD0603-060

Place inductors so that the fields from adjacent filters DO NOT couple.

VDAC_RED

C434 15pF L4 620nH C437 33pF C438 56pF
C435 8.2pF L5 0.82uH C439 56pF
C436 47pF L6 220nH C440 3.3pF

R392 0 EC62 1000uF PR/R

ESD7 ***PESD0603-060

Place inductors & 0 ohm R's so that the fields from adjacent filters DO NOT couple.

16 PB/B
16 Y/G
16 PR/R
16 SVIDEO_C
16 SVIDEO_Y
16 COMP_RCA

VDAC_LUMA

C442 5% 12pF R162 0 C446 33pF (DNI) C447 120pF 5%
C443 5% 1.5pF L7 1.5uH 5% C448 100pF
C445 NI 47pF 5% R163 0 C449 NI 3.3pF

R393 0 EC63 1000uF SVIDEO_C

ESD8 ***PESD0603-060

Place inductors & 0 ohm R's so that the fields from adjacent filters DO NOT couple.

VDAC_CHROMA

C450 5% 12pF R181 0 C453 33pF (DNI) C454 120pF 5%
C451 5% 1.5pF L8 1.5uH 5% C455 100pF
C452 NI 47pF 5% R182 0 C456 NI 3.3pF

R394 0 EC64 1000uF SVIDEO_Y

ESD9 ***PESD0603-060

Place ESD5~7 as close as possible to J19

C457 5% 12pF R183 0 C460 33pF (DNI) C461 120pF 5%
C458 5% 1.5pF L9 1.5uH C462 100pF
C459 NI 47pF 5% R184 0 C463 NI 3.3pF

R395 0 EC65 1000uF COMP_RCA

ESD10 ***PESD0603-060

A5V

BC3 0.1uF BC4 0.1uF BC5 0.1uF BC6 0.1uF BC7 0.1uF BC8 0.1uF BC9 0.1uF BC10 0.1uF

06

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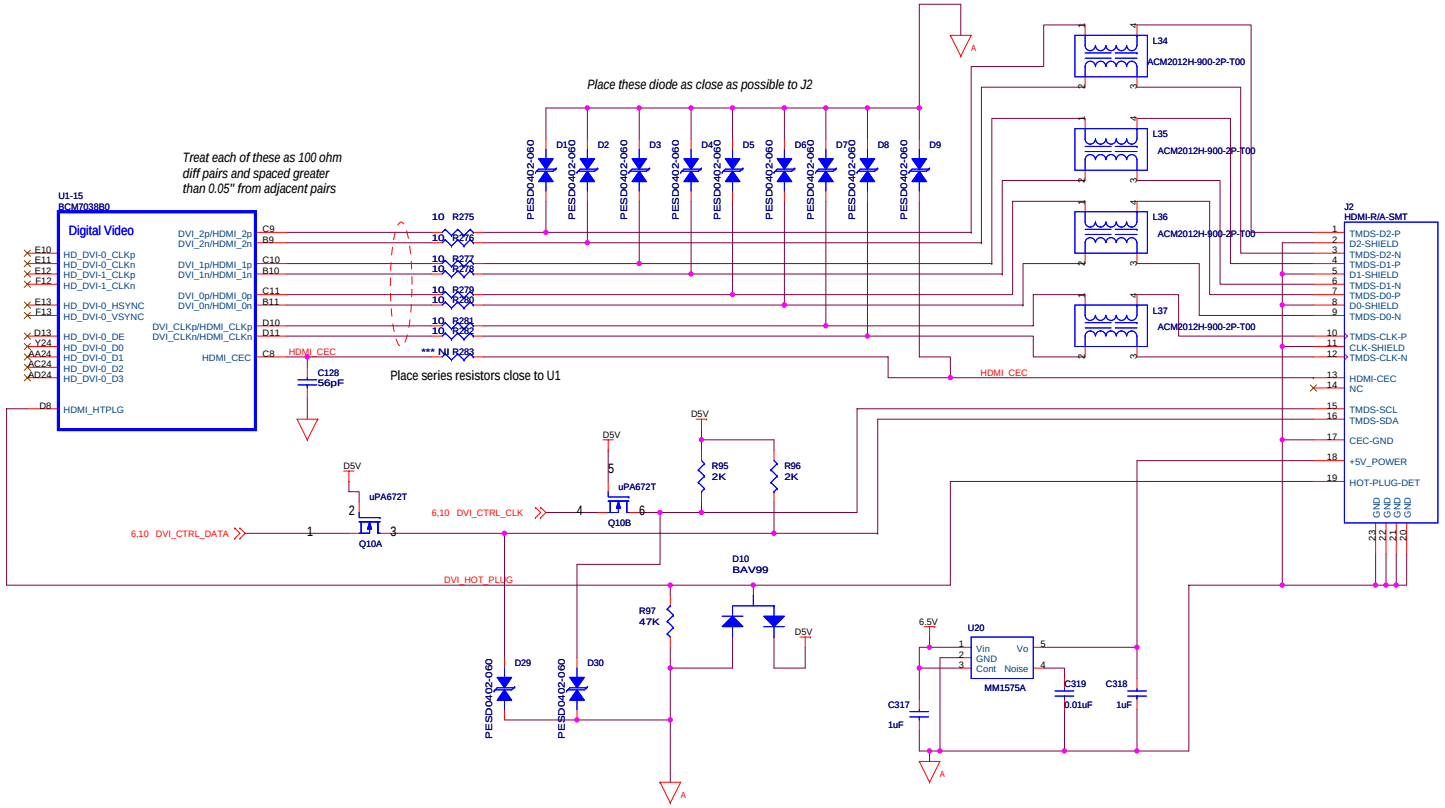
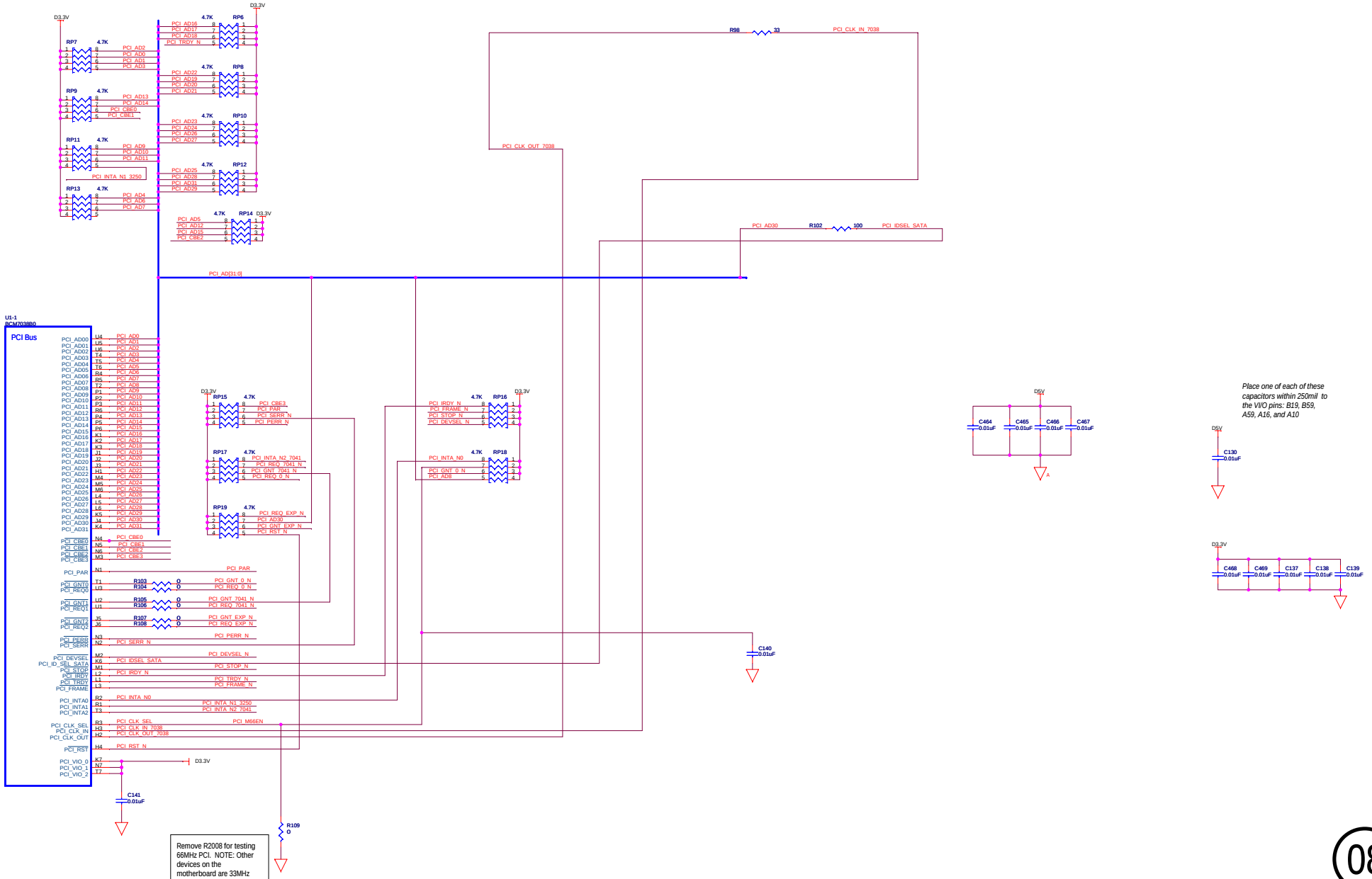
Title: Philips_DVR
Size: C
Document Number: Video DAC output
Rev: 1.1
Date: Monday, April 16, 2007
Sheet 6 of 19



07

ZINWELL CORPORATION [Hsinchu] R&D II		
2, Wen-Hua Road, Hsinchu Industrial Park,Hsinchu 303, Taiwan TEL:886-3-597-9050 # 559		
Title: Philips_DVR		
Size: C	Document Number: HDMI A/V	Rev: 1.1
Date: Monday, April 16, 2007	Sheet 7 of 19	


U1-1
BCM7038B0
PCI Bus
D3.3V
D5V
RP5
RP6
RP7
RP9
RP10
RP11
RP12
RP13
RP14
RP15
RP16
RP17
RP18
RP19
4.7K
PCI_AD[31:0]
PCI_INTA_N1_3250
PCI_CLK_OUT_7038
PCI_CLK_IN_7038
PCI_AD30
R102
100
PCI_IDSEL_SATA
R98
33
C140
0.01uF
C141
0.01uF
R109
0
C464
C465
C466
C467
C130
C468
C469
C137
C138
C139
Place one of each of these capacitors within 250mil to the VI/O pins: B19, B59, A59, A16, and A10
Remove R2008 for testing 66MHz PCI. NOTE: Other devices on the motherboard are 33MHz only PCI agents and must not be accessed when testing in 66MHz mode.
08
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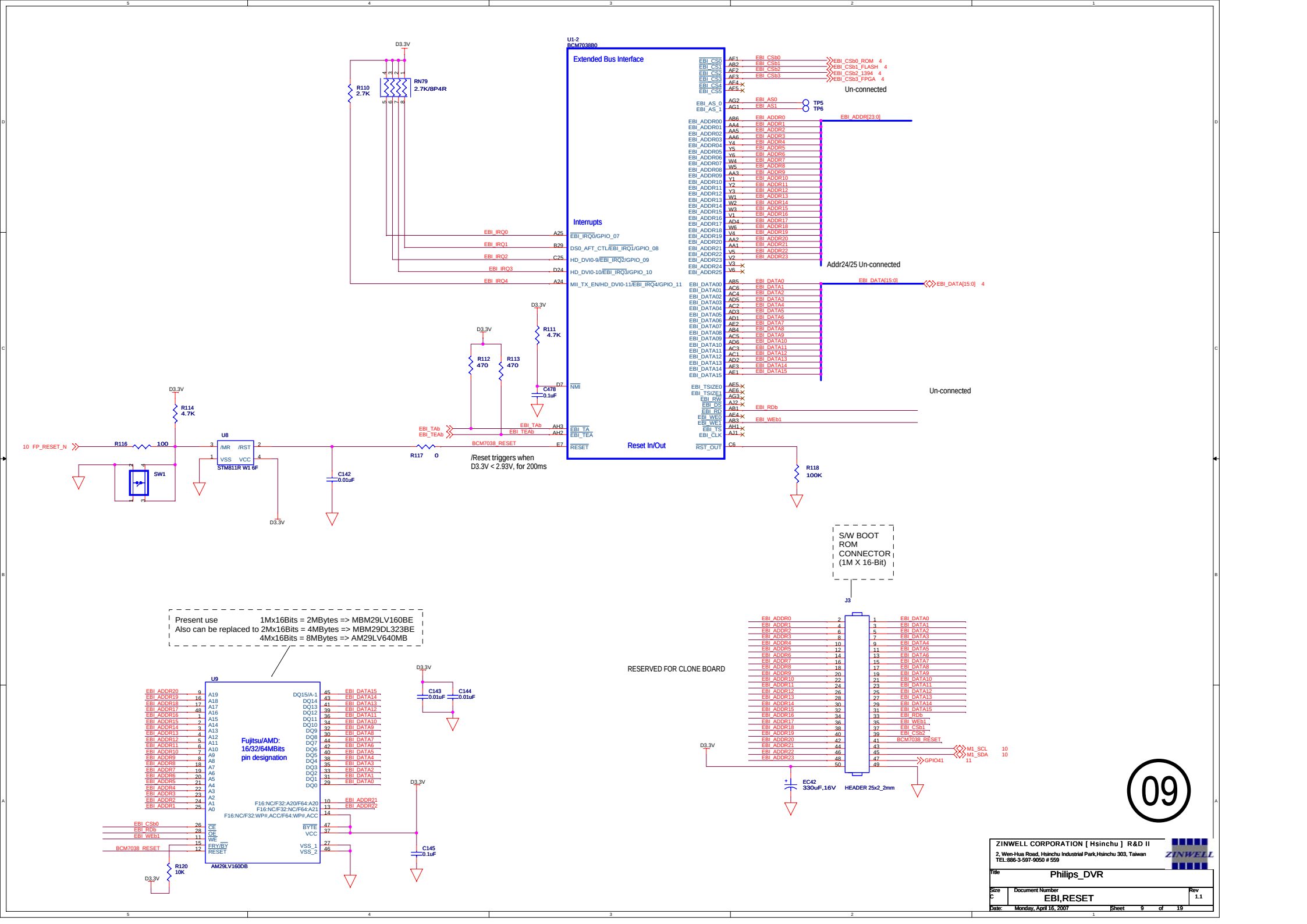
TEL:886-3-597-9050 # 559
Philips_DVR
PCI
Rev 1.1
Monday, April 16, 2007
Sheet 8 of 19


U1-2
BCM7038B0
Extended Bus Interface
Interrupts
Reset In/Out
Un-connected
Addr24/25 Un-connected
Un-connected
R110 2.7K
RN79 2.7K/8P4R
R111 4.7K
R112 470
R113 470
R114 4.7K
R116 100
R117 0
R118 100K
R120 10K
C142 0.01uF
C143 0.01uF
C144 0.01uF
C145 0.1uF
C478 0.1uF
SW1
U8
STM811R W1 6F
/Reset triggers when
D3.3V < 2.93V, for 200ms
S/W BOOT ROM CONNECTOR (1M X 16-Bit)
J3
HEADER 25x2_2mm
EC42 330uF,16V
RESERVED FOR CLONE BOARD
Present use 1Mx16Bits = 2MBytes => MBM29LV160BE
Also can be replaced to 2Mx16Bits = 4MBytes => MBM29DL323BE
4Mx16Bits = 8MBytes => AM29LV640MB
U9
Fujitsu/AMD:
16/32/64MBits
pin designation
AM29LV160DB
09
ZINWELL CORPORATION [Hsinchu] R&D II
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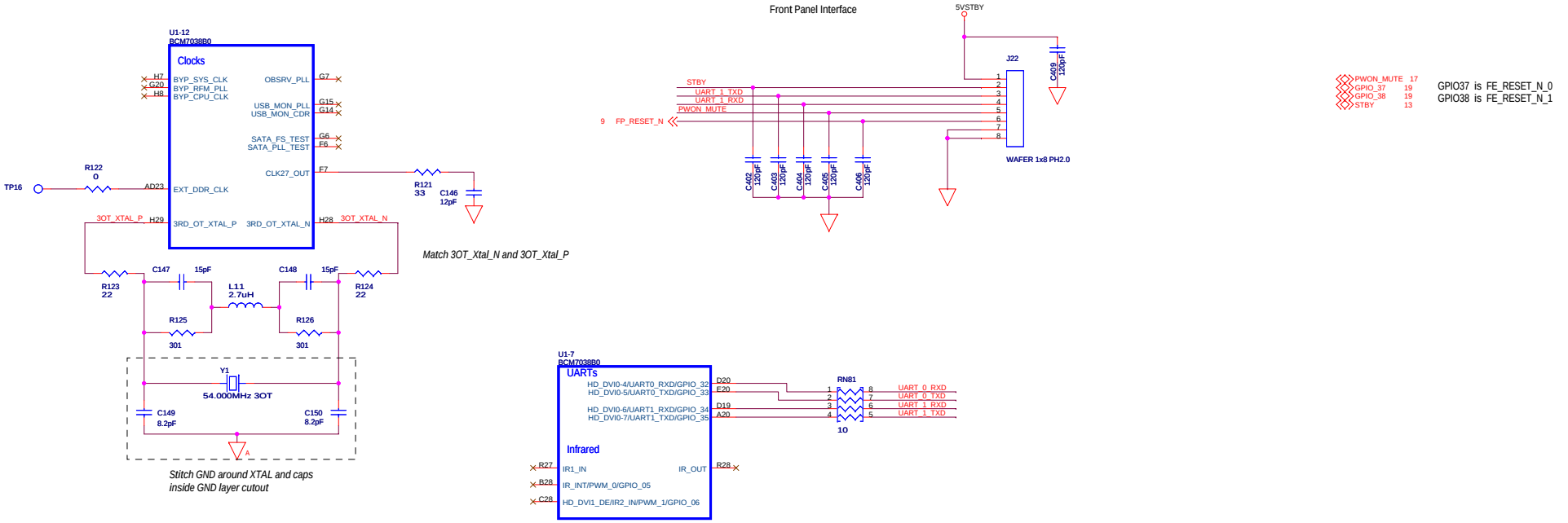
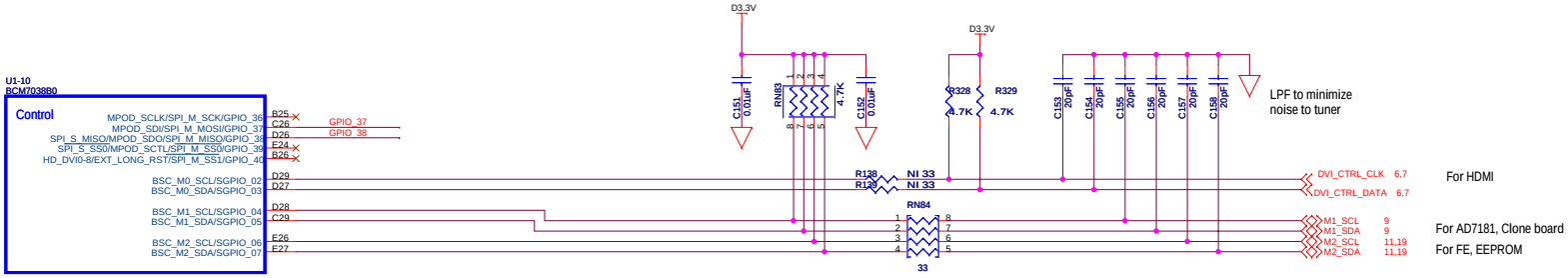
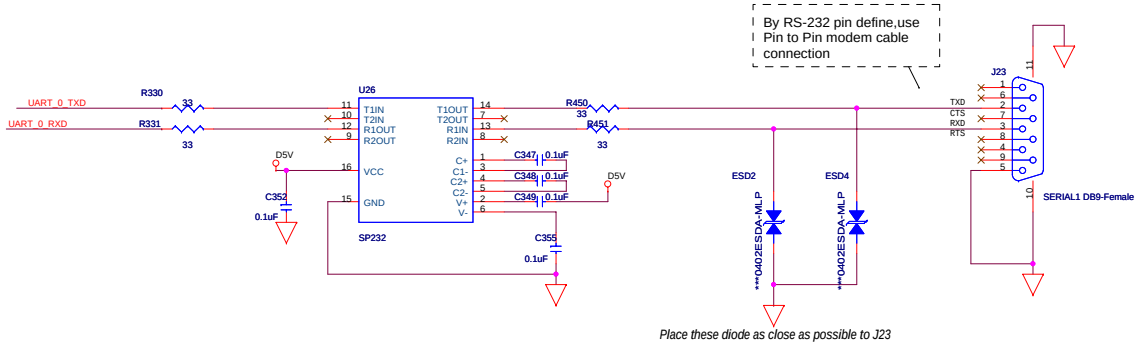
TEL:886-3-597-9050 # 559
Philips_DVR
EBI,RESET
Monday, April 16, 2007
Sheet 9 of 19

Front Panel Interface



Control





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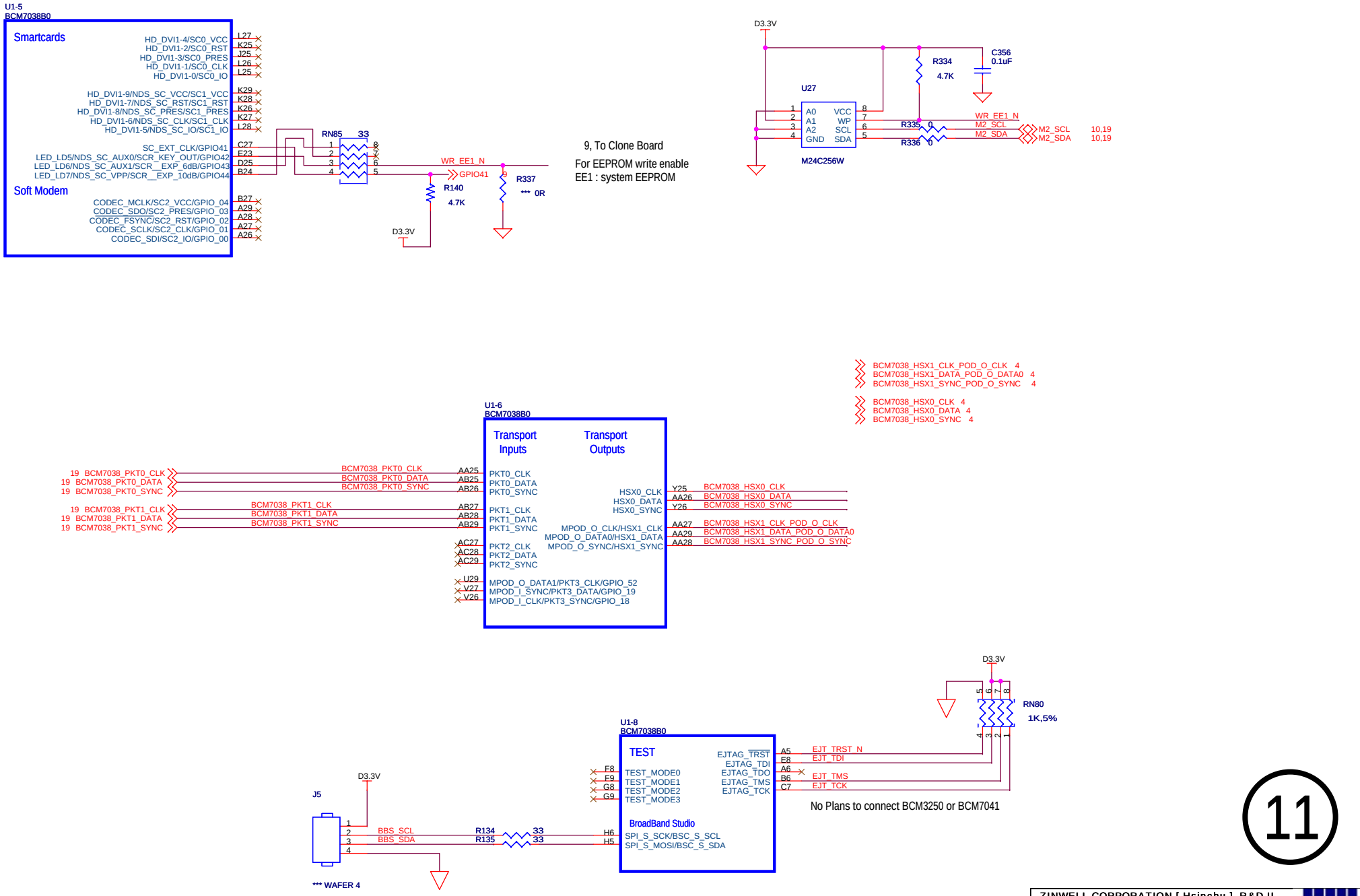
ZINWELL CORPORATION [Hsinchu] R&D II 2, Wen-Hua Road, Hsinchu Industrial Park,Hsinchu 303, Taiwan TEL:886-3-597-9050 # 559		
Title: Philips_DVR		
Size: C	Document Number: BSC,PKT,CLKS	Rev: 1.1
Date: Wednesday, January 24, 2007	Sheet 10 of 19	


U1-5
BCM7038B0
Smartcards
HD_DVI1-4/SC0_VCC
HD_DVI1-2/SC0_RST
HD_DVI1-3/SC0_PRES
HD_DVI1-1/SC0_CLK
HD_DVI1-0/SC0_IO
HD_DVI1-9/NDS_SC_VCC/SC1_VCC
HD_DVI1-7/NDS_SC_RST/SC1_RST
HD_DVI1-8/NDS_SC_PRES/SC1_PRES
HD_DVI1-6/NDS_SC_CLK/SC1_CLK
HD_DVI1-5/NDS_SC_IO/SC1_IO
SC_EXT_CLK/GPIO41
LED_LD5/NDS_SC_AUX0/SCR_KEY_OUT/GPIO42
LED_LD6/NDS_SC_AUX1/SCR__EXP_6dB/GPIO43
LED_LD7/NDS_SC_VPP/SCR__EXP_10dB/GPIO44
Soft Modem
CODEC_MCLK/SC2_VCC/GPIO_04
CODEC_SDO/SC2_PRES/GPIO_03
CODEC_FSYNC/SC2_RST/GPIO_02
CODEC_SCLK/SC2_CLK/GPIO_01
CODEC_SDI/SC2_IO/GPIO_00
RN85
33
WR_EE1_N
GPIO41
R140
4.7K
R337
*** 0R
D3.3V
9, To Clone Board
For EEPROM write enable
EE1 : system EEPROM
U27
M24C256W
A0
A1
A2
GND
VCC
WP
SCL
SDA
R334
4.7K
C356
0.1uF
R335 0
R336 0
WR_EE1_N
M2_SCL
M2_SDA
10,19
BCM7038_HSX1_CLK_POD_O_CLK 4
BCM7038_HSX1_DATA_POD_O_DATA0 4
BCM7038_HSX1_SYNC_POD_O_SYNC 4
BCM7038_HSX0_CLK 4
BCM7038_HSX0_DATA 4
BCM7038_HSX0_SYNC 4
U1-6
BCM7038B0
Transport Inputs
Transport Outputs
PKT0_CLK
PKT0_DATA
PKT0_SYNC
PKT1_CLK
PKT1_DATA
PKT1_SYNC
PKT2_CLK
PKT2_DATA
PKT2_SYNC
MPOD_O_DATA1/PKT3_CLK/GPIO_52
MPOD_I_SYNC/PKT3_DATA/GPIO_19
MPOD_I_CLK/PKT3_SYNC/GPIO_18
HSX0_CLK
HSX0_DATA
HSX0_SYNC
MPOD_O_CLK/HSX1_CLK
MPOD_O_DATA0/HSX1_DATA
MPOD_O_SYNC/HSX1_SYNC
BCM7038_PKT0_CLK
BCM7038_PKT0_DATA
BCM7038_PKT0_SYNC
BCM7038_PKT1_CLK
BCM7038_PKT1_DATA
BCM7038_PKT1_SYNC
BCM7038_HSX0_CLK
BCM7038_HSX0_DATA
BCM7038_HSX0_SYNC
BCM7038_HSX1_CLK_POD_O_CLK
BCM7038_HSX1_DATA_POD_O_DATA0
BCM7038_HSX1_SYNC_POD_O_SYNC
U1-8
BCM7038B0
TEST
TEST_MODE0
TEST_MODE1
TEST_MODE2
TEST_MODE3
EJTAG_TRST
EJTAG_TDI
EJTAG_TDO
EJTAG_TMS
EJTAG_TCK
BroadBand Studio
SPI_S_SCK/BSC_S_SCL
SPI_S_MOSI/BSC_S_SDA
RN80
1K,5%
EJT_TRST_N
EJT_TDI
EJT_TMS
EJT_TCK
No Plans to connect BCM3250 or BCM7041
J5
BBS_SCL
BBS_SDA
R134
R135
33
*** WAFER 4
11
ZINWELL CORPORATION [Hsinchu] R&D II
2, Wen-Hua Road, Hsinchu Industrial Park,Hsinchu 303, Taiwan
TEL:886-3-597-9050 # 559
Title
Philips_DVR
Size
A3
Document Number
EJTAG, TS, EEPROM
Rev
1.1
Date:
Monday, April 16, 2007
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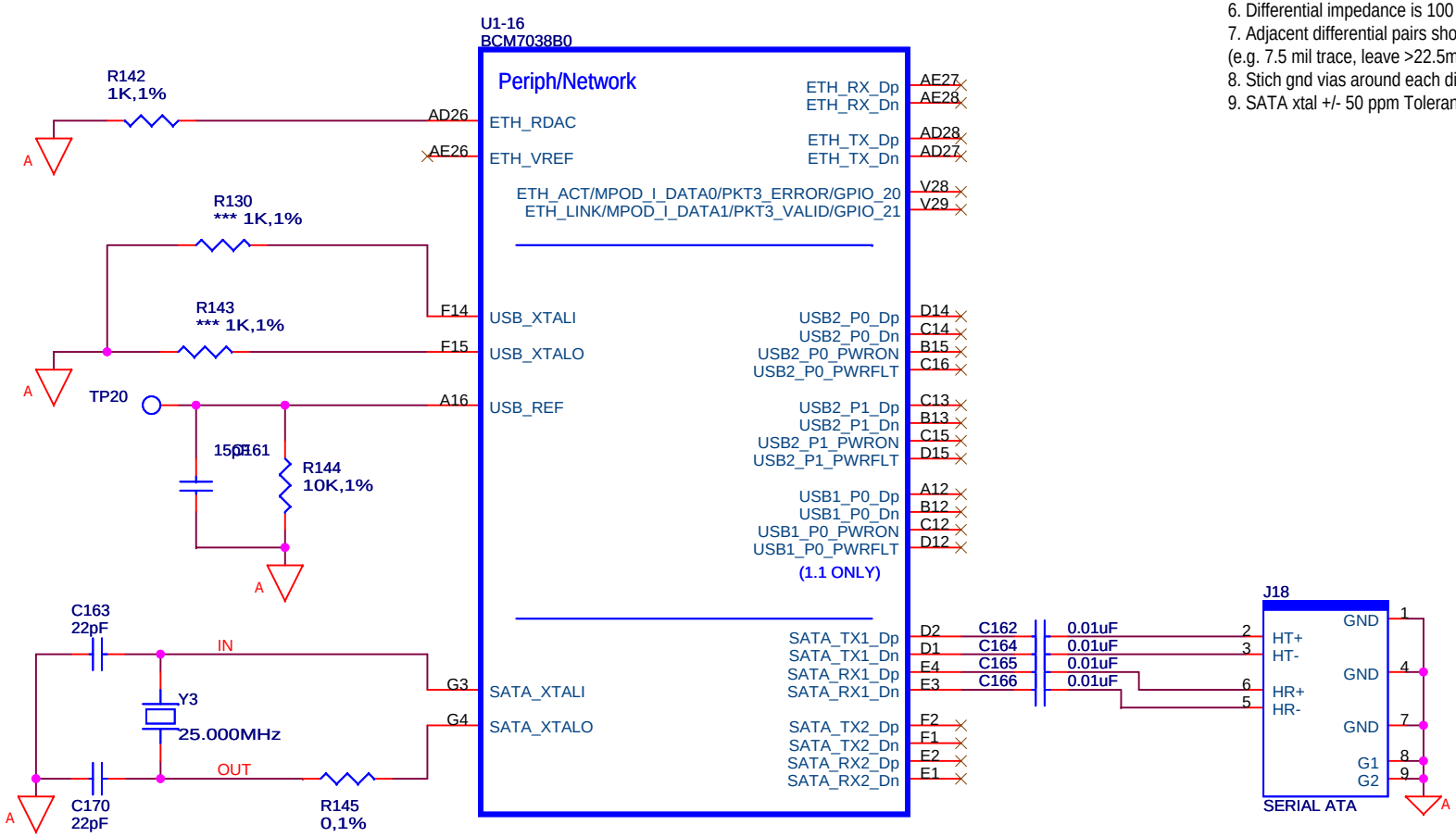
19

Route TXP/M and RXP/M pairs differentially, matched short lengths, with 100 ohm differential impedance, adjacent to ground plane.

SATA & USB - Layout Guidelines & Notes

1. The Dp and Dn traces are length matched, with max differential skew, within 20mils
2. Differential trace length must be less than 5 inches
3. No more than 2 vias per trace, prefer zero.
4. Never split the ground plane under differential pair routing
5. Route differential pairs above the GND plane.
6. Differential impedance is 100 Ohms for SATA and 90 ohms for USB.
7. Adjacent differential pairs should be separated by at least 3 times the trace width. (e.g. 7.5 mil trace, leave >22.5mils between adjacent diff pairs)
8. Stich gnd vias around each differential pair, but NOT between a given pair.
9. SATA xtal +/- 50 ppm Tolerance +/- 100 ppm Stability



Y3 need nearly BCM7038 .Stitch GND around XTAL and caps inside GND layer cutout

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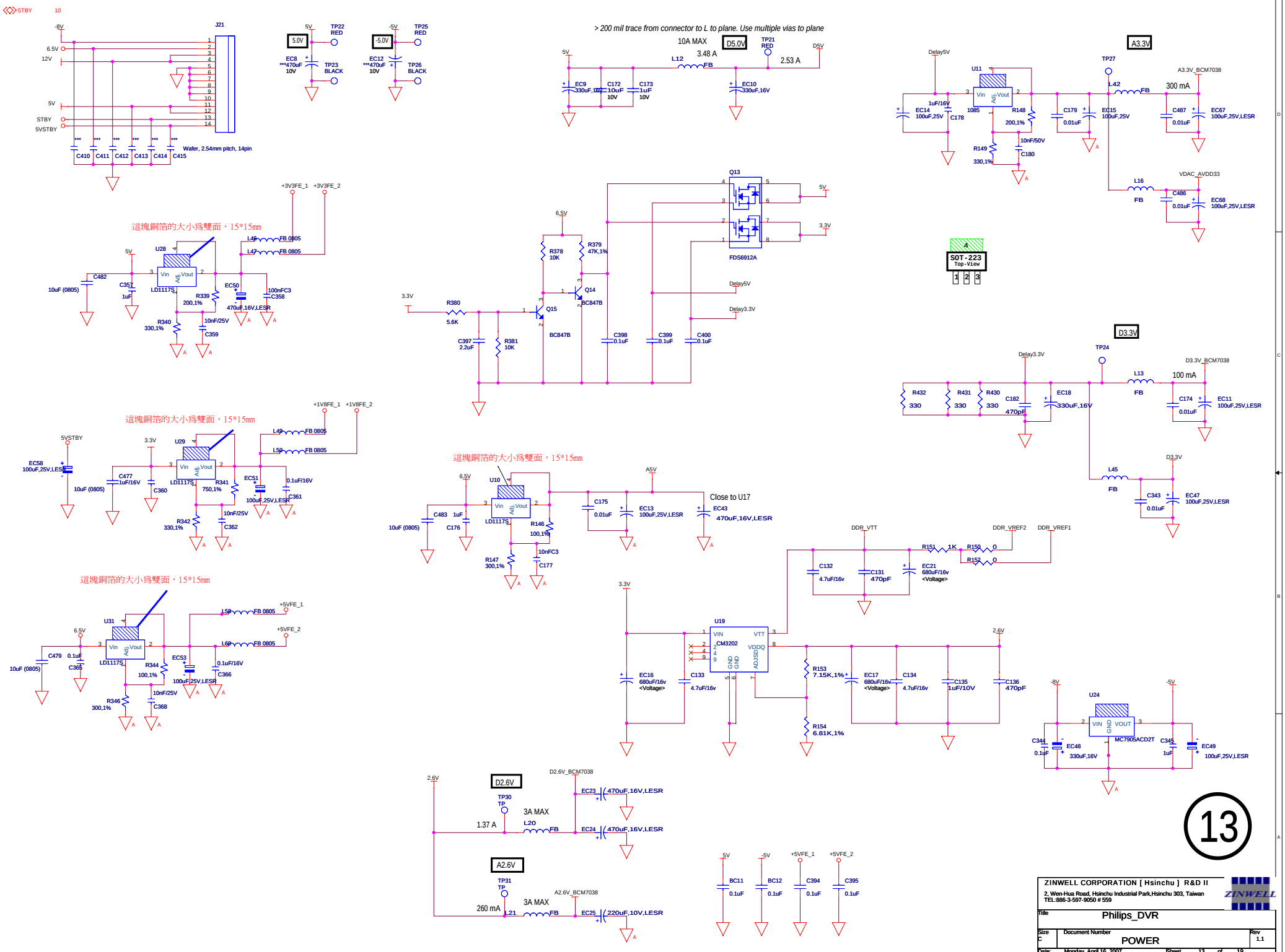
Title	Philips_DVR	
Size A4	Document Number USB;Ethernet;Sata	Rev 1.1
Date: Monday, April 16, 2007	Sheet 12 of 19	


STBY
10
J21
-8V
6.5V
12V
5V
STBY
5VSTBY
Wafer, 2.54mm pitch, 14pin
C410
C411
C412
C413
C414
C415
5.0V
TP22
RED
TP23
BLACK
EC8
470uF
10V
-5.0V
TP25
RED
TP26
BLACK
EC12
470uF
10V
> 200 mil trace from connector to L to plane. Use multiple vias to plane
10A MAX
D5.0V
TP21
RED
D5V
3.48 A
2.53 A
L12
FB
EC9
330uF,16V
C172
10uF
10V
C173
1uF
10V
EC10
330uF,16V
A3.3V
Delay5V
U11
LD1085
Vin
Adj
Vout
EC14
100uF,25V
1uF/16V
C178
R148
200,1%
R149
330,1%
10nF/50V
C180
C179
0.01uF
EC15
100uF,25V
TP27
L42
FB
A3.3V_BCM7038
300 mA
C487
0.01uF
EC67
100uF,25V,LESR
L16
FB
VDAC_AVDD33
C486
0.01uF
EC68
100uF,25V,LESR
+3V3FE_1
+3V3FE_2
這塊銅箔的大小爲雙面，15*15mm
U28
LD1117S
L46
FB 0805
L47
FB 0805
C482
10uF (0805)
C357
1uF
R339
200,1%
EC50
470uF,16V,LESR
100nFC3
C358
R340
330,1%
10nF/25V
C359
Q13
FDS6912A
R378
10K
R379
47K,1%
Q14
BC847B
Q15
BC847B
R380
5.6K
C397
2.2uF
R381
10K
C398
0.1uF
C399
0.1uF
C400
0.1uF
Delay5V
Delay3.3V
SOT-223
Top-View
D3.3V
Delay3.3V
TP24
D3.3V_BCM7038
100 mA
L13
FB
C174
0.01uF
EC11
100uF,25V,LESR
R432
330
R431
330
R430
330
C182
470pF
EC18
330uF,16V
L45
FB
D3.3V
C343
0.01uF
EC47
100uF,25V,LESR
+1V8FE_1
+1V8FE_2
這塊銅箔的大小爲雙面，15*15mm
5VSTBY
EC58
100uF,25V,LESR
10uF (0805)
U29
LD1117S
C477
1uF/16V
C360
L49
FB 0805
L50
FB 0805
R341
750,1%
EC51
100uF,25V,LESR
0.1uF/16V
C361
R342
330,1%
10nF/25V
C362
這塊銅箔的大小爲雙面，15*15mm
U10
LD1117S
C483
1uF
C176
R146
100,1%
R147
300,1%
10nFC3
C177
C175
0.01uF
EC13
100uF,25V,LESR
A5V
Close to U17
EC43
470uF,16V,LESR
這塊銅箔的大小爲雙面，15*15mm
U31
LD1117S
+5VFE_1
+5VFE_2
L58
FB 0805
L60
FB 0805
C479
0.1uF
C365
R344
100,1%
EC53
100uF,25V,LESR
0.1uF/16V
C366
R346
300,1%
10nF/25V
C368
DDR_VTT
DDR_VREF2
DDR_VREF1
R151
1K
R150
0
R152
0
C132
4.7uF/16v
C131
470pF
EC21
680uF/16v
<Voltage>
U19
CM3202
VIN
VTT
VDDQ
GND
GND
ADJSD
C133
4.7uF/16v
EC16
680uF/16v
<Voltage>
R153
7.15K,1%
R154
6.81K,1%
EC17
680uF/16v
<Voltage>
C134
4.7uF/16v
C135
1uF/10V
C136
470pF
2.6V
U24
MC7905ACD2T
VIN
GND
VOUT
C344
0.1uF
EC48
330uF,16V
C345
1uF
EC49
100uF,25V,LESR
D2.6V
TP30
TP
3A MAX
1.37 A
L20
FB
D2.6V_BCM7038
EC23
470uF,16V,LESR
EC24
470uF,16V,LESR
A2.6V
TP31
TP
260 mA
L21
FB
A2.6V_BCM7038
3A MAX
EC25
220uF,10V,LESR
BC11
0.1uF
BC12
0.1uF
C394
0.1uF
C395
0.1uF
13
ZINWELL CORPORATION [Hsinchu] R&D II
2, Wen-Hua Road, Hsinchu Industrial Park,Hsinchu 303, Taiwan
TEL:886-3-597-9050 # 559
ZINWELL
Title
Philips_DVR
Size
C
Document Number
POWER
Rev
1.1
Date:
Monday, April 16, 2007
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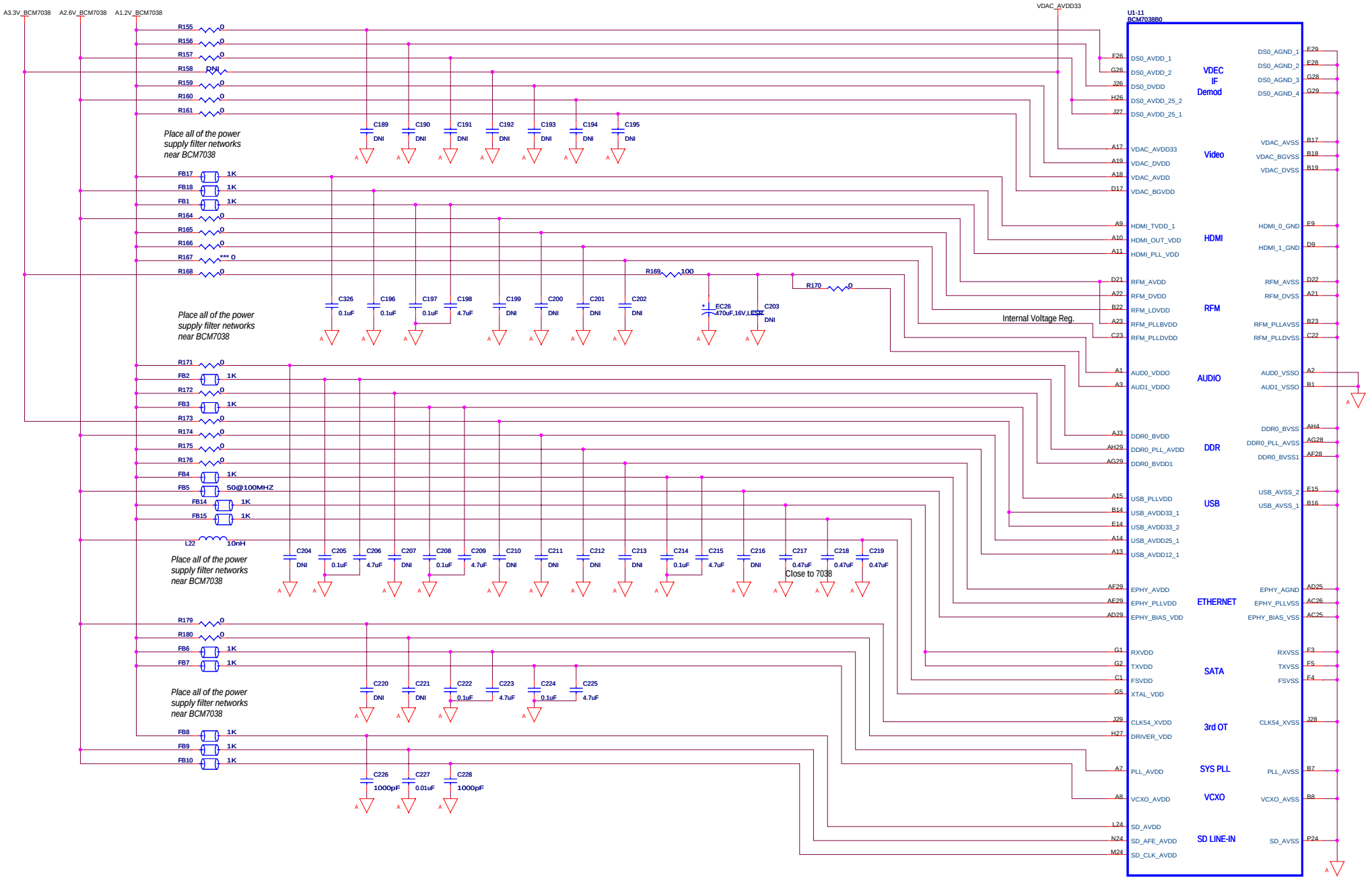
13
of
19



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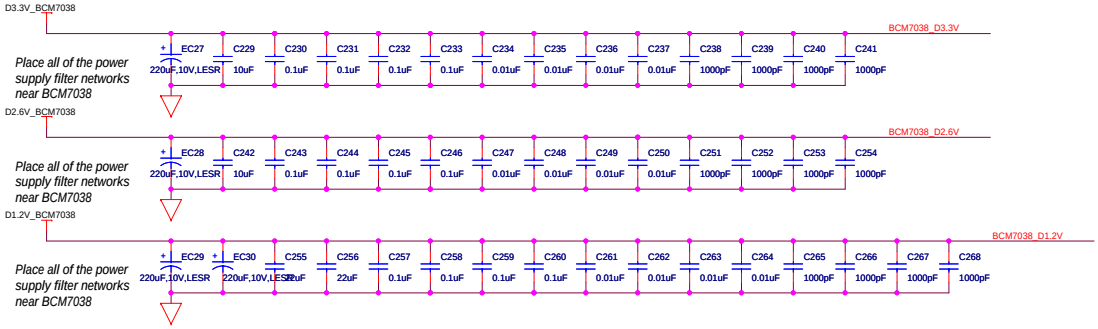
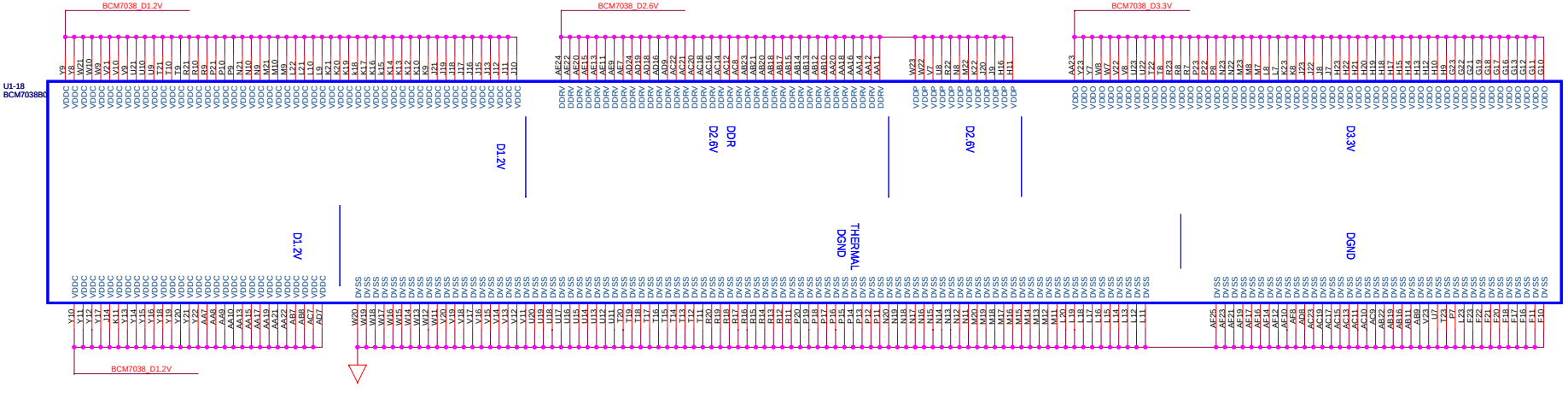
ZINWELL

Title: Philips_DVR

Size: C | Document Number: Analog Decoupling | Rev: 1.1

Date: Monday, April 16, 2007 | Sheet 14 of 19





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ZINWELL CORPORATION [Hsinchu] R&D II
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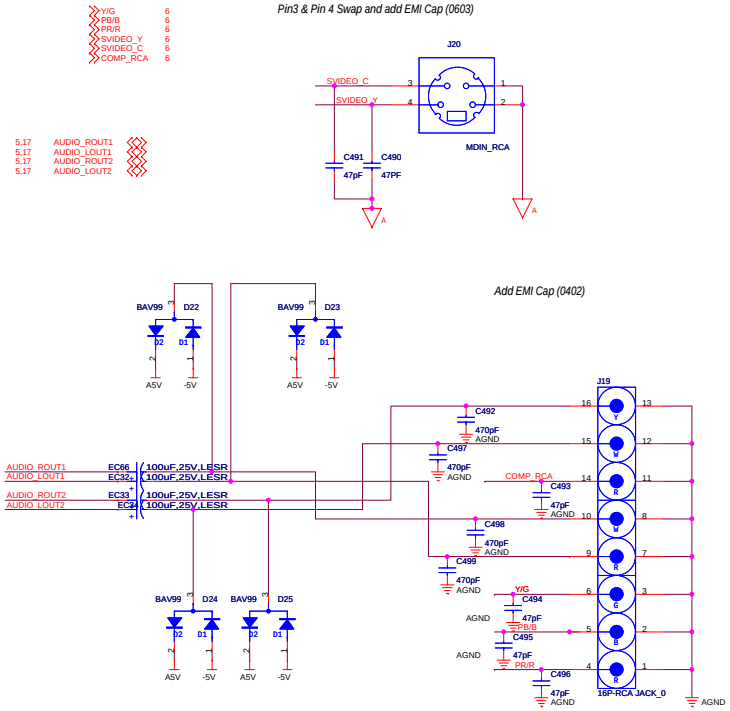
TEL:886-3-597-9050 # 559

Title	Philips_DVR	
Size C	Document Number: Digital Decoupling	Rev 1.1
Date: Monday, April 16, 2007	Sheet 15 of 19	



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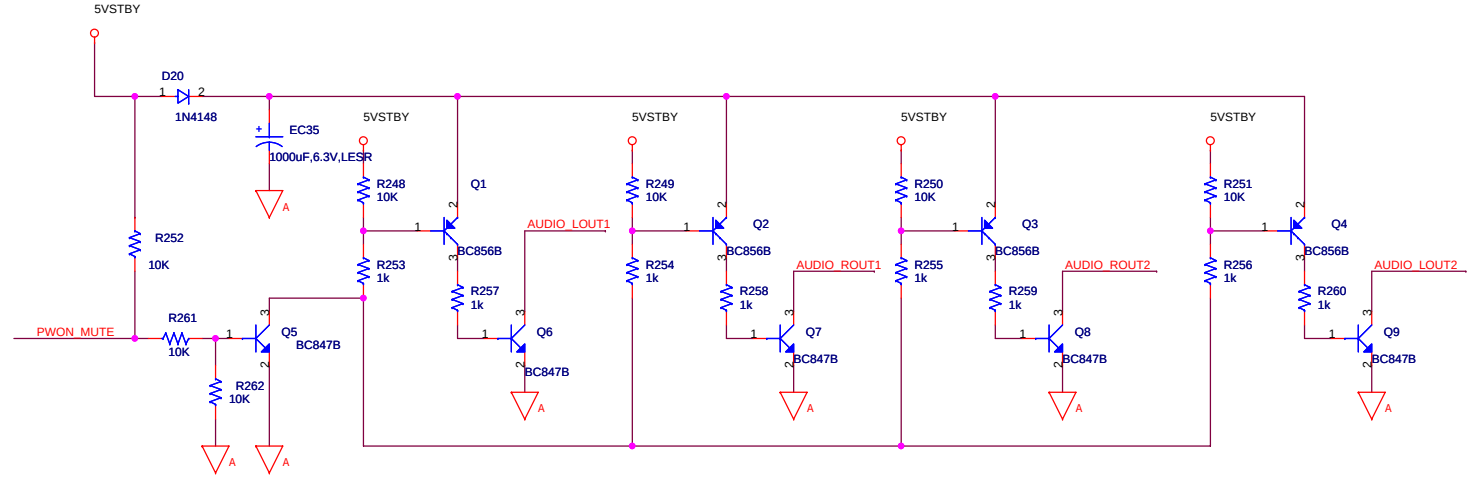
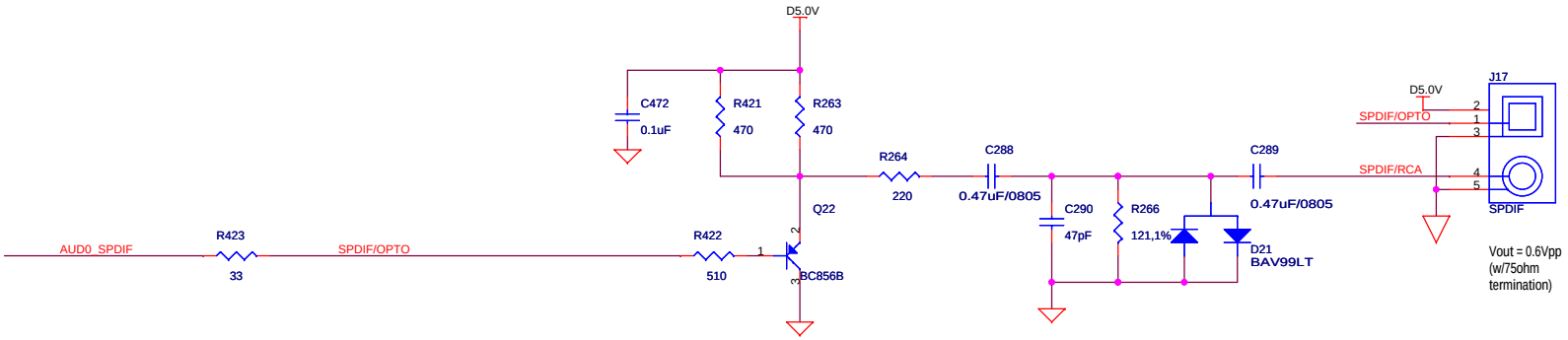
ZINWELL CORPORATION [Hsinchu] R&D II

2, Wen-Hua Road, Hsinchu Industrial Park,Hsinchu 303, Taiwan
TEL:886-3-597-9050 # 559

Title: Philips_DVR		
Size: A2	Document Number: Video Buffers	Rev: 1.1
Date: Monday, April 16, 2007	Sheet 16 of 19	

5 AUD0_SPDIF
5,16 AUDIO_ROUT1
5,16 AUDIO_LOUT1
5,16 AUDIO_ROUT2
5,16 AUDIO_LOUT2
10 PWON_MUTE





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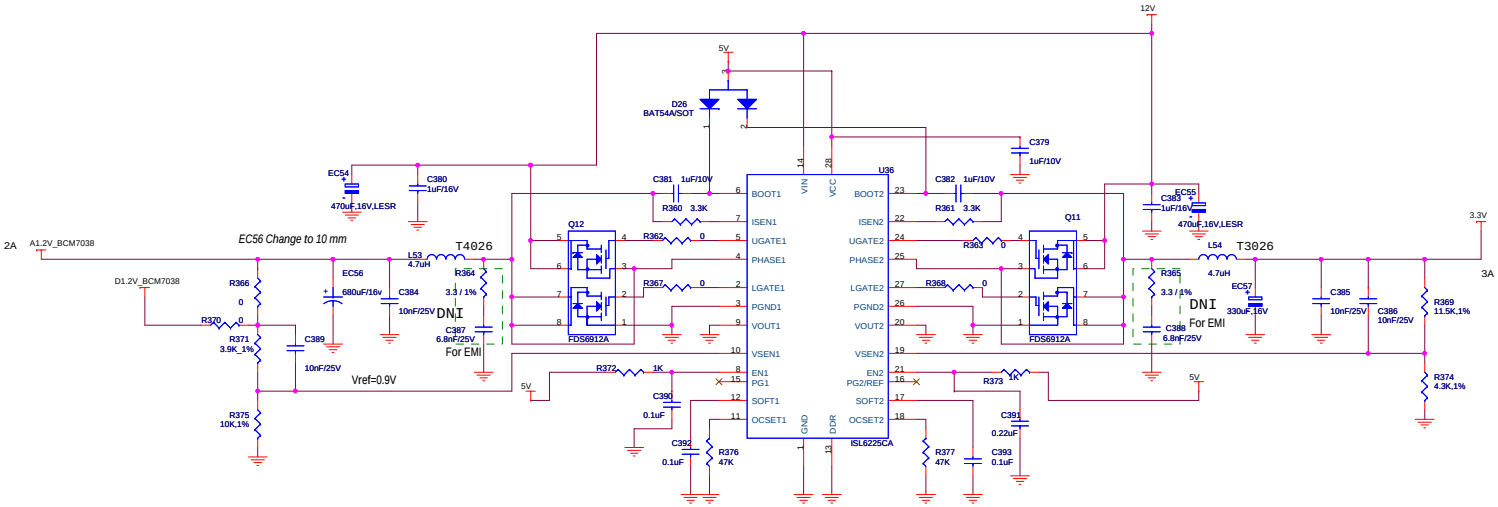
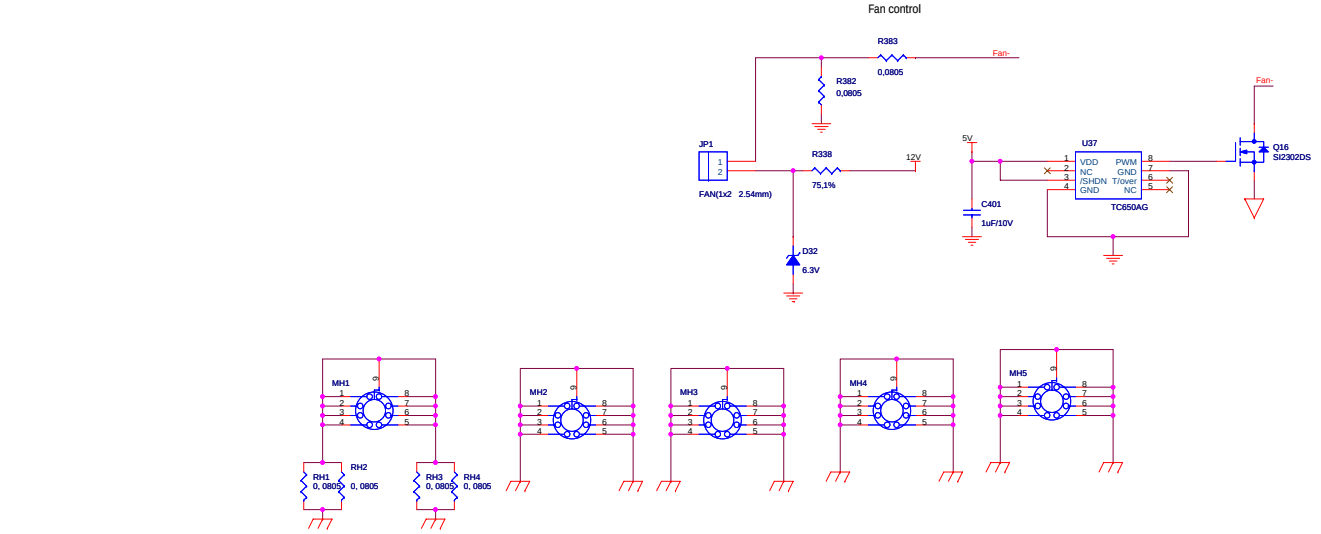
ZINWELL CORPORATION [Hsinchu] R&D II
2, Wen-Hua Road, Hsinchu Industrial Park,Hsinchu 303, Taiwan
TEL:886-3-597-9050 # 559

Title	Philips_DVR	
Size A3	Document Number: Audio Connection	Rev 1.1
Date: Monday, April 16, 2007	Sheet 17 of 19	





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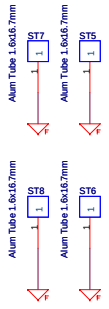
ZINWELL CORPORATION [Hsinchu] R&D II
2, Wen-Hua Road, Hsinchu Industrial Park,Hsinchu 303, Taiwan
TEL:886-3-597-9050 # 559

Title: Philips_DVR

Size: A2 | Document Number: DC-DC Converter & Fan control | Rev: 1.1

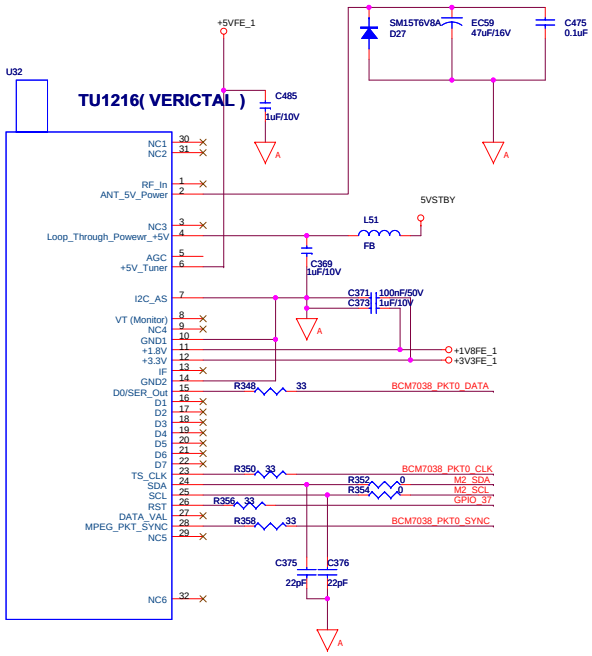
Date: Monday, April 16, 2007 | Sheet 18 of 19

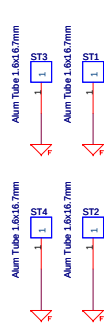


Place side by tuner U32

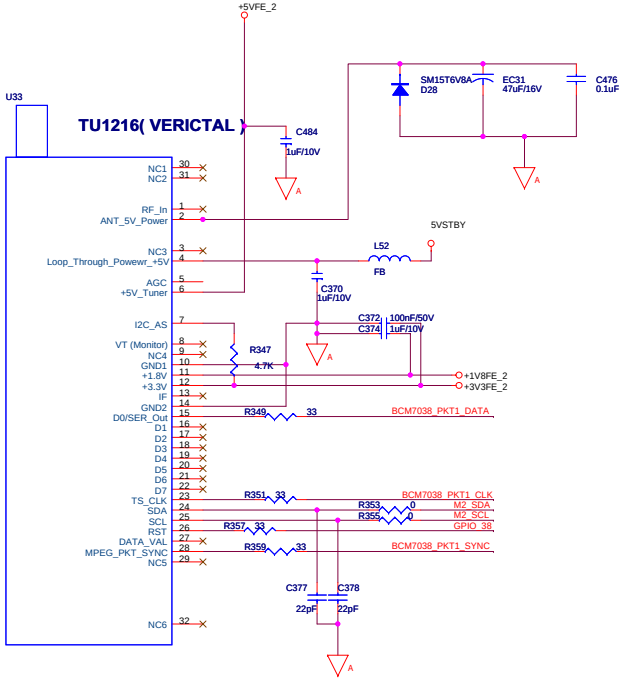
GPIO37 is FE_RESET_N_0
GPIO38 is FE_RESET_N_1

GPIO_37 10
GPIO_38 10
BCM7038_PKT0_CLK 11
BCM7038_PKT0_DATA 11
BCM7038_PKT0_SYNC 11
BCM7038_PKT1_CLK 11
BCM7038_PKT1_DATA 11
BCM7038_PKT1_SYNC 11
M2_SCL 10,11
M2_SDA 10,11





Place side by tuner U33



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